

# High–Conversion Ratio Multi-Phase VRM Realized with Generic Modular Series-Capacitor Boost Cells

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**Abstract**—This paper introduces a high–conversion ratio multi-phase non-isolated DC–DC topology built from generic series-capacitor boost cells. Using a stand-alone  $LC$  cell, the approach contributes to a high modularity of the resulting converters and enables high conversion ratios. The unique interaction between the capacitor and the inductor results in a soft-charging operation, which curbs the losses of the converter and contributes to higher efficiency. The method was used to create a multi-phase step-up DC–DC module for microinverters. The new converter significantly extends the effective duty ratio and lowers the voltage stress of the transistors. In addition, it has inherent current sharing to balance the load between the phases. Experimental results of a modular interleaved two-phase prototype demonstrate an excellent proof of design methodology concept and agree well with the simulations and theoretical analyses developed in this study.

**Keywords**—DC–DC power converters, high conversion ratio, microinverters, series-capacitor boost converter, voltage regulator module.

## I. INTRODUCTION

Over the past few years, the renewable energy sector has experienced remarkable growth, with a significant increase in the capacity of renewable energy sources worldwide. As the world moves toward sustainable energy solutions, renewables account for approximately 20% of global energy consumption, including nearly 30% of electricity generation [1]. Solar power has seen impressive progress, with its contribution to global electricity generation rising from 1% in 2015 to 4% in 2021 [2]. This expansion has been made possible by the advancements in key components such as photovoltaic (PV) inverters, which play a crucial role in connecting solar panels to the grid or directly to the load in stand-alone systems.

Microinverters are gaining significant popularity in residential applications and capturing an increasing market share. This is primarily due to their compact size, plug-and-play concept, ease of installation and maintenance, and ability to deliver higher power yields even under partial shading conditions. However, microinverters face a unique challenge—they require a substantial voltage boost to match the input PV voltage, which typically ranges from 20–40 V DC, to the grid voltage of 120 V / 230 V AC.

Two major approaches are commonly used to implement microinverters. One proposed method involves a single-switching stage [3]–[6]. The single-stage microinverter configuration utilizes a single PV with a single DC–AC block consisting of a transformer, coupled inductor, switch capacitors, or a combination of these. Another approach uses two switching stages. The two-stage power processing [7]–[10] consists of a DC–DC step-up converter in series with a DC–AC inverter, as illustrated in Fig. 1.

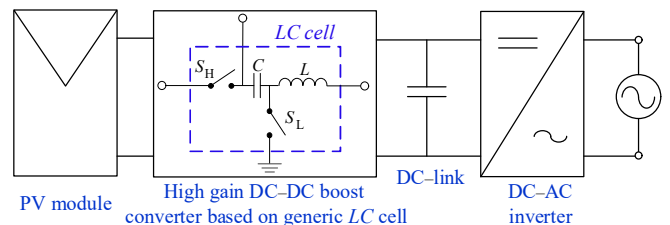


Fig. 1. Microinverter implementation with two switching stages: DC–DC and DC–AC. The DC–DC stage is based on a generic  $LC$  cell for a modular multi-phase boost converter.

Numerous microinverter applications have been extensively studied and documented in the literature [11]–[23]. Typical applications involve isolated converters, which employ high-frequency transformers to achieve significant voltage step-up through turns ratio accommodation. However, these conventional isolated implementations suffer drawbacks, such as high cost, large size, and reduced efficiency due to bulky transformers. To address these limitations, non-isolated microinverters have emerged, offering smaller form factors, lower costs, and improved efficiency. Nevertheless, non-isolated designs must carefully manage high voltage stresses on the switches to maintain overall system efficiency.

The objective of this study is to introduce a regulated modular multi-phase, non-isolated DC–DC topology for very high conversion ratios and high-power applications with high efficiency. The core concept of this new topology, depicted in Fig. 2, revolves around using generic  $LC$  cells with optimal design guidelines that can easily meet the industry requirements for a wide range of applications, making microinverters an excellent use case for this novel approach. This topology effectively triples the duty ratio (in the case of two cells), lowers and better distributes the transistors' voltage stress, and features natural current sharing between the phases. This paper discusses and analyzes the DC–DC stage of the microinverter and expands the studies published in [24] and [25] with a demonstration of step-up topology.

The rest of the paper is organized as follows. Section II presents the operation principle of a two-phase of series-capacitor boost converter and provides typical key waveforms of the new converter. In Section III, a full steady-state analysis of the converter is delineated. Simulation and experimental results are provided in Section IV, and Section V concludes the paper.

## II. MULTI-PHASE SERIES CAPACITOR BOOST CONVERTER

The development of a generic  $LC$  cell as a basic building block is shown in Figs. 1 and 2. The cell includes one inductor, one capacitor, and two switches that are driven in a complementary method. Multiple cells can be connected for

current sharing and energy processing. This unique approach of designing with a generic cell allows the extension of any desired number of phases, with the benefits of higher duty-ratio resolution, significantly lower voltage stress on the switches, and inherent current balancing [26]–[28], making this multi-phase topology an ideal candidate for high-conversion ratio applications.

Throughout the paper, the concept is presented and analyzed on a two-phase topology, named as double series-capacitor boost converter (DSCBOC), as illustrated in Fig. 2(a). The DSCBOC topology combines the benefits of a switched-capacitor circuit and a series-capacitor boost converter [10]. The connection between cells is achieved by connecting all inductor inputs to the input source and the high side (voltage level) of the flying capacitor from one cell to the high-side switch ( $S_{xH}$ ) of the next cell. An additional switch is used to connect the high-side point of the flying capacitor from the latest cell to the low-side switch ( $S_{xL}$ ) of the previous cell.

To simplify the explanation of the circuit operation of the multi-phase topology described in Fig. 2(a), assume that the output capacitor  $C_o$  and flying capacitors  $C_1$  and  $C_2$  are large and the voltage ripple across them are relatively small compared to their DC voltages. The description of the DSCBOC operation is aided by the idealized timing diagram in Fig. 2(b) and the sub-circuits with their currents paths highlighted in Fig. 3. The switching period is divided into four time intervals with four states (I–IV), where states II and IV are identical, functioning as “balance” states.

During state I, switches  $S_{1H}$  and  $S_{2L}$  are ON [i.e., phase 1 is OFF, and phase 2 is ON; see Fig. 3(a)]. In addition, capacitor  $C_1$  and inductor  $L_1$  are discharging to the load, where the input source is also connected. Throughout this state, inductor  $L_2$  is charged from the input source, where the inductor is connected between GND and the input source. In states II and IV, switches  $S_{1L}$  and  $S_{2L}$  are ON [phases 1 and 2 are ON; see Fig. 3(b)], where inductors  $L_1$  and  $L_2$  are connected to GND in one node and to the input source in the second node. As a result, the two phases are ON, and the inductors currents are charged from the input source. In state III, switches  $S_{1L}$  and  $S_{2H}$  are ON [phase 1 is ON, and phase 2 is OFF; see Fig. 3(c)]. In addition, capacitor  $C_1$  is charged by the input source and through inductor  $L_2$  and capacitor  $C_2$ , which are discharged, i.e., the stored energy in the  $L_2$  and  $C_2$  is delivered to capacitor  $C_1$ . Inductors  $L_1$  and  $L_2$  are phase-shifted 180 degrees from each other in the two-cells implementation. Note that in the case of a boost converter, high-side switches  $S_{1H}$ ,  $S_{2H}$ , and  $S_{1-2}$  can be implemented with diodes. This can reduce the complexity of using floating drivers.

### III. STEADY STATE ANALYSIS

The steady-state analysis of the DSCBOC topology presented in this section is assisted by a steady-state simulation of a 400 W, 20-to-400 V converter, operating at 200 kHz switching frequency per phase, as depicted in Figs. 2 and 4.

#### A. Conversion Ratio

The analysis of the DSCBOC is based on the inductor-voltage second balance of each phase and the current second

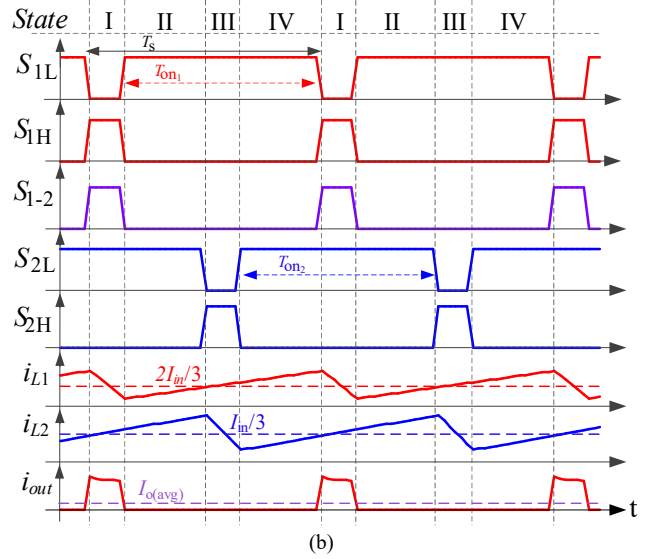
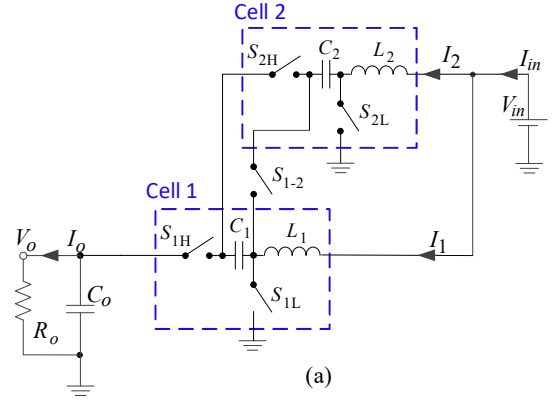


Fig. 2. Double series-capacitor boost converter. (a) Circuit diagram of two cells. (b) Timing diagram and idealized waveforms of DSCBOC topology.

balance of the output capacitor  $C_o$ . The following are the inductors equations from each switching state. Equalizing inductors current ripples for their ON and OFF intervals can be expressed as

$$\Delta i_{L1} = \frac{V_{in}}{L_1} D_1 T_s \Big|_{\text{Charge}} = - \left\{ \frac{V_{in} - (V_o - V_{C1})}{L_1} (1 - D_1) T_s \right\} \Big|_{\text{Dis.}} \quad (1)$$

$$\Delta i_{L2} = \frac{V_{in}}{L_2} D_2 T_s \Big|_{\text{Charge}} = - \left\{ \frac{V_{in} - (V_{C1} - V_{C2})}{L_2} (1 - D_2) T_s \right\} \Big|_{\text{Dis.}} \quad (2)$$

where  $L_1$  is charging during states II, III, and IV and discharged at state I, and  $L_2$  is charging during states I, II, and IV and discharged at state III. In addition,  $D_1$  and  $D_2$  are the ON time for each phase, respectively. Without losing generality, assuming equal inductance values and substituting  $V_{C2}$  for  $V_o - V_{C1}$ , a system of two linear equations and two unknowns can be written as

$$\begin{cases} V_{C2} = \left[ 1 + \frac{D_1}{1 - D_1} \right] V_{in} \\ V_{C1} - V_{C2} = \left[ 1 + \frac{D_2}{1 - D_2} \right] V_{in} \end{cases} \quad (3)$$

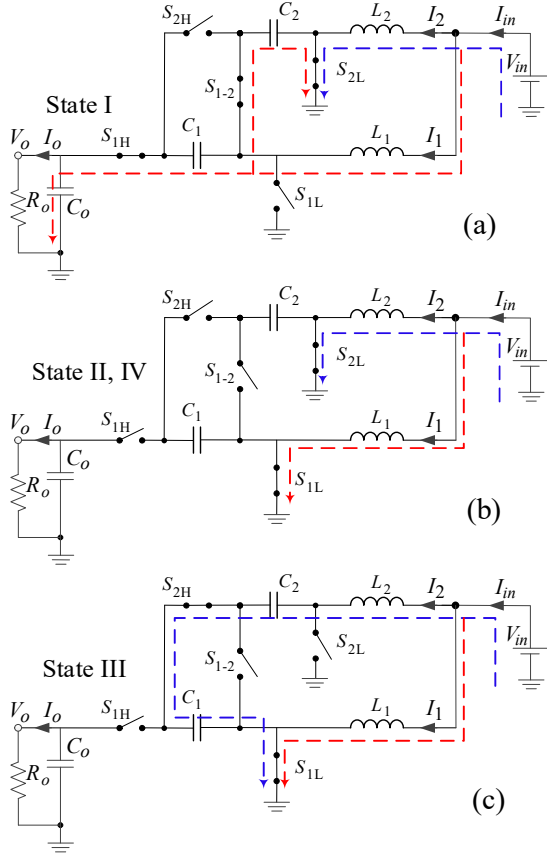


Fig. 3. Operation states I-IV. (a) State I: phase 1 is OFF, and phase 2 is ON. (b) States II and IV: both phases are ON. (c) State III: phase 2 is OFF, and phase 1 is ON.

Solving the system yields the average capacitors voltages:

$$V_{C1} = 2 \left[ \frac{1}{1-D_1} \right] V_{in}, \quad V_{C2} = \left[ \frac{1}{1-D_2} \right] V_{in}. \quad (4)$$

The voltage conversion ratio can be derived from (3) and (4), and by setting equal duty ratios, i.e.,  $D_1=D_2=D$ , the conversion ratio  $M$  can be expressed as

$$M = \frac{V_{out}}{V_{in}} = 3 \left[ \frac{1}{1-D} \right], \quad (5)$$

which is three times higher than the duty ratio of a typical boost converter. In this case, the average capacitors voltages as functions of the output voltage are  $V_{C1} = 2V_o/3$  and  $V_{C2} = V_o/3$ .

### B. Stress on Switches

The average voltages of all switches at steady state are summarized in Table I, which shows the switch stresses of each state for one switching cycle. As can be shown, the presence of the flying capacitors is the main key for reducing the stress on each MOSFET and can be reduced further with more cells. The resulting voltage stress is significantly lower compared to conventional boost converters. In traditional multi-phase boost topologies, the maximum stress equals the output voltage. Another comparison is with similar studies published in [8] and [10], where reducing the stress to the same level as in the proposed topology can be obtained by adding more phases.

TABLE I.

SWITCHES VOLTAGES OF EACH STATE IN THE DSCBOC CONVERTER

Switch	State/Stress			
	I	II	III	IV
$S_{1L}$	$V_{C2}$	0	0	0
$S_{1H}$	0	$V_o - V_{C1}$	$V_o - V_{C1}$	$V_o - V_{C1}$
$S_{1-2}$	0	$V_{C2}$	$V_{C1}$	$V_{C2}$
$S_{2L}$	0	0	$V_{C1} - V_C$	0
$S_{2H}$	$V_{C1}$	$V_{C1} - V_C$	0	$V_{C1} - V_C$

### C. Inductor Currents and Balancing

The converter's input current analysis can be calculated based on the input capacitor, where  $i_{in} = C_{in}(dV_{in}/dt)$ , and by the fact that at steady state, the average capacitor current is zero. Taking the current second balance of the capacitor and the absolute slew rate of the input capacitor current during charging and discharging, the following equation can be written as

$$I_{C_{in}} \Big|_{\text{Charge}} = (I_{L1} + I_{L2}) \Big|_{\text{Discharge}}. \quad (6)$$

The average value of each inductor current at steady state can be calculated considering the charge balance is achieved for each capacitor [29], [30]. For example, the charge delivered to  $C_2$  during state I must equal the charge consumed from  $C_2$  (by  $C_1$ ) during state III. This yields

$$Q_{C1} : I_{L2} \frac{D_2}{f_s} \Big|_{\text{Charge (state III)}} = \frac{1}{2} I_{L1} \frac{D_1}{f_s} \Big|_{\text{Discharge (state I)}},$$

$$Q_{C2} : \frac{1}{2} I_{L1} \frac{D_1}{f_s} \Big|_{\text{Charge (state I)}} = I_{L2} \frac{D_2}{f_s} \Big|_{\text{Discharge (state III)}}. \quad (7)$$

Solving the system using (6) yields the average inductor currents:

$$I_{L1} = \frac{2D_2}{D_1 + 2D_2} I_{in}, \quad I_{L2} = \frac{D_1}{D_1 + 2D_2} I_{in}. \quad (8)$$

Therefore, in the private case, setting equal duty ratios  $D_1=D_2=D$  for the two phases results in average inductor currents of  $I_{L1} = 2I_{in}/3$  and  $I_{L2} = I_{in}/3$ . From the equations, phase 1 has double the current than phase 2 caused by the discharge of inductor  $L_2$  and capacitor  $C_2$  at state III. The ratio between the average inductors currents can be written as

$$\frac{I_{L1}}{I_{L2}} = \frac{2D_2}{D_1}. \quad (9)$$

The inductor current balance between phases is achieved by setting the duty cycle of phase 2 to half that of phase 1. As a result, the average inductor currents are  $I_{L1} = I_{L2} = I_{in}/2$ . Note that the voltage ratio of the converter is affected by implementing a current balance between phases.

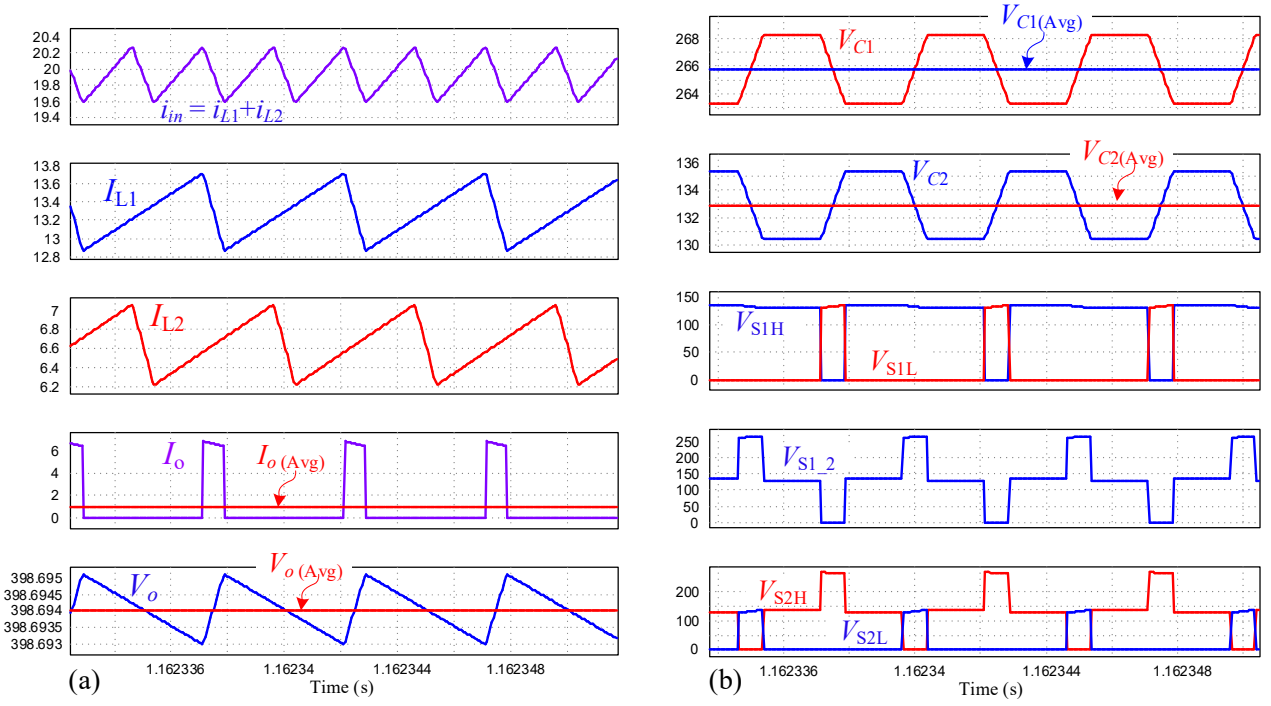


Fig. 4 Simulation results of DSCBOC single module;  $M = 20$ . (a) Output voltage, inductors currents, and input and output currents, where all duty cycles are equal. (b) Voltages across the flying capacitors  $V_{C1}$  and  $V_{C2}$  and voltages across all switches,  $S_{1L}$ ,  $S_{1H}$ ,  $S_{1-2}$ ,  $S_{2L}$ , and  $S_{2H}$ .

#### D. CCM–DCM Boundary

The DSCBOC converter is implemented in continuous current mode (CCM). The general formula for the boundary between CCM to discontinuous mode (DCM) is given in (10), where the inductors currents  $I_{L1,2(\min)}$  are set to zero [31]–[33]. The formula represents the average inductors currents one step before moving to DCM mode, where the inductors current goes to zero at the end of the off period, that is,

$$I_{L1,2\min} = 0 = I_{L1,2(av)} + \frac{\Delta i_{L1,2}}{2}. \quad (10)$$

The average inductor currents can be determined from the input current using (5) and by output power after neglecting the system loss:

$$V_{in} I_{in} = \frac{(3V_m/1-D)^2}{R_o}. \quad (11)$$

Substituting (8) and (11) into (10) and after some manipulation,  $I_{L1\min}$  can be written as

$$I_{L1\min} = \frac{2}{3} \left( \frac{9V_{in}}{(1-D)^2 R_o} \right) - \left( \frac{V_{in} D / L_1}{2f_s} \right) = 0. \quad (12)$$

The boundary between CCM to DCM modes can be expressed as

$$L_{1\min} = \frac{D(1-D)^2 \cdot R_o}{12f_s}, \quad (13)$$

where  $L_{1(\min)}$  is the minimum inductance required for operating in CCM mode,  $f_s$  is the switching frequency, and  $R_o$  is the load resistance. Inductor  $L_{2\min}$  can be calculated with a similar method, as follows:

$$L_{2\min} = \frac{(1-D)^2 D \cdot R_o}{6f_s}. \quad (14)$$

#### IV. SIMULATION AND EXPERIMENTAL RESULTS

The verification and proof-of-concept demonstration of the design methodology is carried out by a simulation and experiment of a two-phase series-capacitor boost converter.

Fig. 4 shows the steady-state simulation of a 400 W, 20-to-400 V converter operating at 200 kHz switching frequency per phase. The simulation shows the key waveforms of the new topology. Fig. 4(a) demonstrates the output voltage, inductors currents, and the sum of the inductors currents, i.e. input current. From the results, natural current sharing occurs between phases with a ratio of 2:1 between  $I_{L2}$  to  $I_{L1}$ . Fig. 4(b) shows the voltages of the flying capacitors  $V_{C1}$  and  $V_{C2}$  and the voltage stresses across all switches,  $S_{1L}$ ,  $S_{1H}$ ,  $S_{1-2}$ ,  $S_{2L}$ , and  $S_{2H}$ . This simulation with a ratio of  $M = 20$  is carried out to demonstrate an extreme case of the conversion ratio.

The DSCBOC prototype operating at a switching frequency of 100 kHz per phase was built and tested, as shown in Fig. 5. Table II lists the component values and nominal parameters of the experimental prototype. Each cell consisted of one MOSFET for the low side of the voltage level, one diode on the high side, one inductor, and one flying capacitor. The converter's power stage included two 270  $\mu$ H inductors and two 3.13  $\mu$ F ceramic capacitors. Each flying capacitor is constructed from six 4.7  $\mu$ F capacitors, where two lines of three series capacitors were connected in parallel to reduce the voltage stress on each capacitor and lower the ESR. A microchip dsPIC33 controller generated the low-side switches  $S_{1L}$  and  $S_{2L}$ .

Fig. 6 shows the experimental results, in which Fig. 6(a) demonstrates the inductors and output currents waveforms and Fig. 6(b) shows the measurements of the input voltage, output voltage, and the series-capacitor voltages at  $M = 12$ . Fig. 7 shows the measured voltages on switches that are in good agreement with Table I. The measured efficiency is demonstrated in Fig. 8(a) for two voltage ratios,  $M = 6$  and 12.

Other experiments were carried out with a wide input voltage range of 5–40 V, a voltage ratio of  $M = 10$ , and a maximum power of 212 W, as shown in Fig. 8(b). These experiments demonstrate the case of partial shading of the PV.

TABLE II.  
EXPERIMENTAL PROTOTYPE PARAMETERS

Power Stage		
Component	P/N	Value/Type
Input voltage $V_{in}$		5–40 V
Output voltage $V_{out}$		50–300 V
Switching frequency $f_{sw}$		100 kHz per phase
Input capacitor $C_{in}$		22 $\mu$ F, 450 V
Output capacitor $C_{out}$		1000 $\mu$ F, 450 V
Inductors $L_1, L_2$	PCV-2-274-10L	270 $\mu$ H, 7.2 A
Capacitors $C_1, C_2$	CNA6P1X7R2A475K250AE	4.7 $\mu$ F, 100 V
Power diodes	D10L20U	200 V, 10A
MOSFETs ( $R_{DS(on)}$ )	IRFP250	200 V, 73m $\Omega$
Driver		
Driver (low side)	MIC4427	Dual 1.5A peak
Digital Section		
Microcontroller	dsPIC33FJ16GS502	16-bit, 40 MIPS
Buffer	MC74HCT244AN	

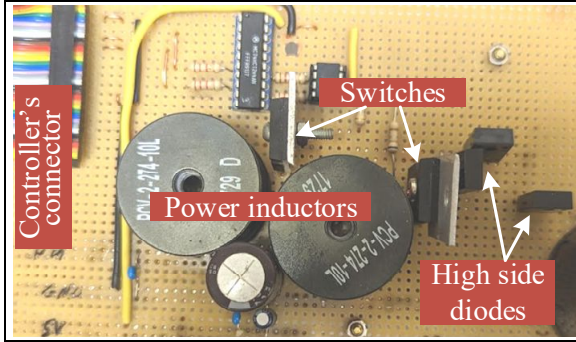


Fig. 5. Prototype of the DSCBOC, a top view of the power stage, which includes the microcontroller bus, power inductors, switches, and high-side diodes.

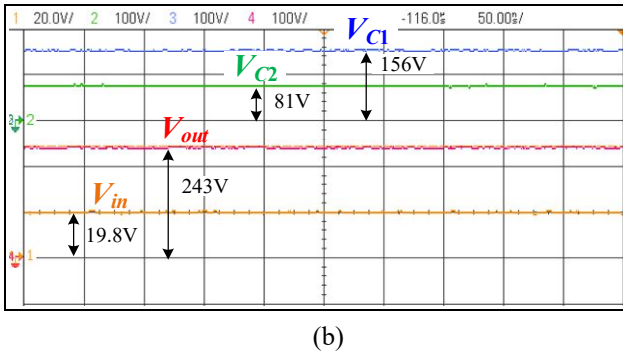
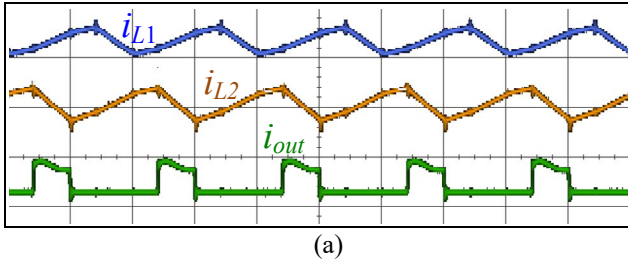


Fig. 6. Experimental results. (a) Inductors and output currents waveforms: blue -  $i_{L1}$ , orange -  $i_{L2}$ , green - output current. Phases are interleaved by 180 degrees. (b) Input voltage (20 V/div), output voltage (100 V/div),  $C_1$  and  $C_2$ —series capacitors voltages (100 V/div).

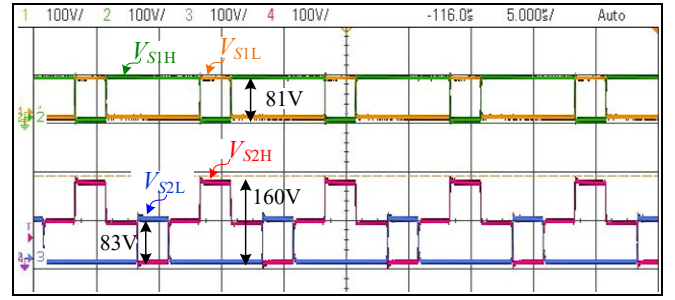


Fig. 7. Experimental results of the switches voltages at  $M = 12$  and input voltage of 20 V.  $S_{1L}$  vs.  $S_{1H}$  (100 V/div) and  $S_{2L}$  vs.  $S_{2H}$  (100 V/div).

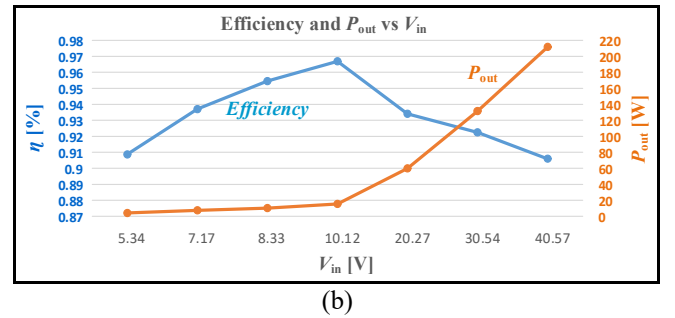
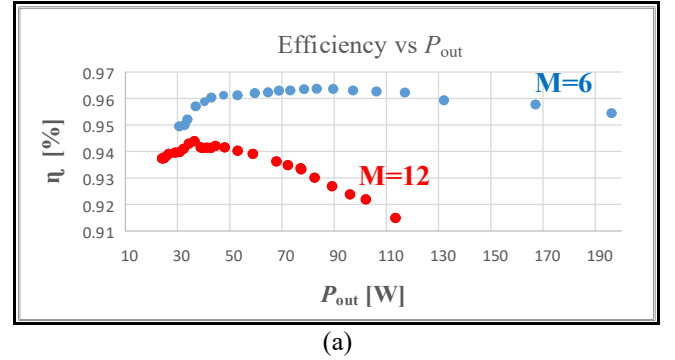


Fig. 8. Experimental results. (a) Measured efficiency:  $V_{in} = 20$  V,  $M = 12$  in red and  $V_{in} = 40$  V,  $M = 6$  in blue. (b) Measured efficiency and output power for a wide range of input voltages of 5–40 V, with a constant voltage ratio of  $M = 10$ .

## V. CONCLUSIONS

A modular series-capacitor boost topology is demonstrated. It comprises multiple phases and uses series capacitors operated in a soft-charging mode. The introduction of series capacitors and their operation in a soft-charging mode lowers the voltage stress of the transistors significantly, extends the duty ratio considerably, and provides an inherent current sharing between the phases. The experimental study of an interleaved two-phase modular prototype demonstrates the behavior, which is in excellent agreement with the simulation and theoretical analysis. The new design methodology, where identical  $LC$  cells comprising inductors and capacitors are used to construct an  $n$ -stage converter, can be effective for various applications, such as the first stage of a microinverter. This technique significantly reduces the complexity of the design and implementation of switched-mode power converters for multiple use cases. Any conversion ratio can be achieved seamlessly and efficiently.

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