Interleaving Boost Extender Topology

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***Abstract* – An efficient first stage interleaving technique for Boost Extender topology is presented. A unique single conversion operation of the boost extender topology, and current stress distribution between the modules pose a challenge on creating a successful and efficient interleaving scheme with this converter. A mechanism is developed, where a supporting first stage in a multilevel high voltage gain structure is added. The supporting stage shares the high current stress of the first boosting stage, compatible with interleaving technique, which reduces the ripples of each inductor along with the input and first stage output capacitor ripples. In addition, the voltage multiplication modules are shared between the interleaved stages providing significant component reduction comparing to traditional interleaving schemes. The concept was validated on a 260W experimental laboratory prototype. Theoretical predictions well agree with simulation and experimental results.**

Keywords –Interleaving, Boost Extender, Boost Capacitor, High voltage gain, Single-switch, Switched capacitor.

I. INTRODUCTION

High voltage gain, and high density non-isolated dc/dc power converter are the most widely adopted converters for the many industrial applications such as uninterruptible power system, communication power system, photovoltaic system and grid connected systems [1],[2]. Literature survey reports many single switch and single power stage high step - up dc/dc converter [3]-[5], to full fill the demand of power converter over a wide load range. A family of high gain boost converter topologies that employed magnetic isolation such as coupled inductor and transformer is introduced to achieve high step -up conversion [6]-[8]. However, due to the resonance effect formed by the coupled inductor and the parasitic capacitors of the diode, these converters require an extra snubber circuitry [9] to absorb the voltage ringing across the diode, which makes it unsuitable for higher power level. In addition, these converters feature a large input current ripple. To overcome some of these deficiencies, interleaving the converters is used to increase the power processing capability. Interleaved converters offer improved dynamic response, reduced magnetic component size and better efficiency comparing to their non-interleaved counterpart. Several high step-up interleaved boost converters are found in literature [10]-[12]. Unfortunately, conventional interleaved boost converter has a limitation on the voltage gain it can provide. One option to alleviate it is an interleaved boost converter that employs switch capacitor cell to increase the gain [13]. Another option is to utilize-cross-coupled inductors as proposed in articles [14] which shows high step-up voltage conversion. Furthermore, the active clamp scheme is utilized to recycle the leakage energy and to supress the voltage spike caused by leakage inductance of the converter. Unfortunately, the three windings structure for the converter make the magnetics and the circuitry rather complex to design.

This paper presents a new interleaved configuration (Fig. 1) that builds on top of a boost extender topology [15], which is capable to increase the voltage gain linearly as the number of extension modules increase. The major challenge with this topology is the increase in the first stage current, which rises proportionally to the number of voltage gain modules. To overcome this challenge, interleaving scenarios are explored in this work, and an interleaved scheme is proposed to share the current stress between the interleaving components, while maintaining overall low component count. The rest of the paper is organized as follows: Section II presents technique for first stage inductor current stress reduction of boost extender, Section III presents the working principle of basic interleaved boost extender converter (Fig. 1), section IV demonstrates the simulation results, section V shows experimental validation of the approach, and conclusions are drawn in section VI.

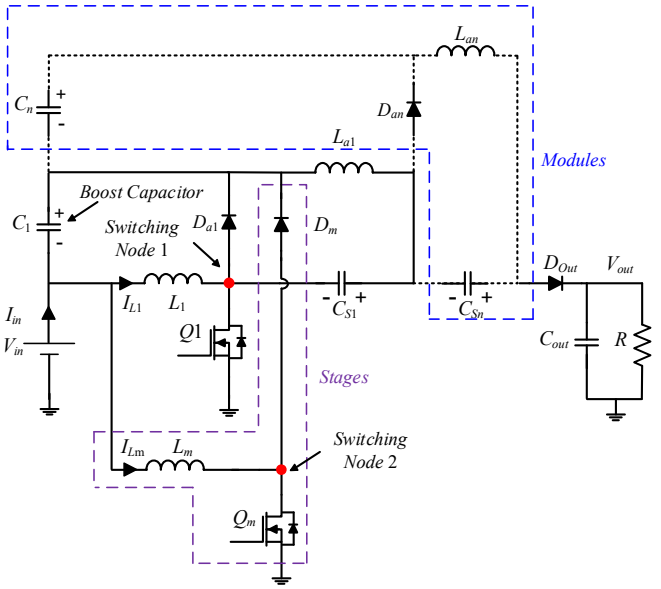

Figure 1: Interleaved Boost extender topology.

II. Boost Inductor Current Stress Reduction Techniques

The boost extender topology of [15] hinges on the stacking of series capacitors, to achieve high voltage gain along with high efficiency. However, once we increase the number of voltage gain modules of the boost extender, it results in input current increase as well, according to the relation of Eq. 1,

$$\frac{V_{out}}{V_{in}} = \frac{1+nD}{1-D} \tag{1}$$

where n is the number of modules and D is duty ratio. This high input current stress is one of the major challenges with high gain boost extender topology. High input current ripple and high current stress create a significant strain on both the first stacked auxiliary capacitor C_1, and the main inductor, which are also referred to as the boost capacitor and the boost inductor, since they are part of the first stage of the boost extender, which operates in the same manner as the regular boost converter. On the contrary the average currents that are flowing through the rest of the extension modules components are relatively minor comparing to the first stage, which creates a huge disbalance in component size and stresses, between the first stage and the rest of the modules. In order to address this issue, some boost extender interleaving options are explored in this work.

The conventional way of interleaving includes exact copies of the whole converter such as in [16]-[18] for boost extender. In this case several independent boost extender circuits are interleaved in a parallel fashion (Fig. 2a) and the input current, as much as the output current are shared by several converters. The downside of this approach, in the case of boost extender, is that in this converter the largest number of components is located within the voltage extension modules that aren't prone to high stresses and majorly underutilized [19]. As a result, interleaving the whole converter including its underutilized extension modules is a significant space and component waste, that pushes further the figure of underutilization of the modules.

A better alternative would be to add in parallel to the first stage some extra inductor-switch pairs to share the high stresses of the first stage only, and utilize a single instance of extension modules. This solution is shown in Fig. 2b. Fig. 2b describes a case where the main inductor and the switch are split into a smaller paralleled inductors and switches. In this case the operation of the converter remains the same, and paralleled switches and inductors are operated in phase with the same duty cycle to share the same current, splitting stress and size requirements for each of the components. It could be beneficial when space constraints are tight, and several smaller components are preferred over a single large one, or when it is impractical to find a single component that withstands the stress. The downside of this approach is that there is no functional advantage to this paralleling scheme, since the overall stress remains the same, and converter size reduction minor to none.

Interleaving the converter shown in Fig. 2b is potentially the best way to overcome the downsides presented in both solutions above. However, the connection of two inductors in parallel and switching them out of phase creates a potential undesired path for the currents to flow from the source through the inductors and to the ground. It happens when any of the interleaving stage switches are conducting in parallel. One way to avoid it is to limit the duty cycle of each phase according to the number of phases and maintain a dead time between all the switches. For example, for two phases the limit would be 50% duty cycle. This approach however is impractical, since the converter is supposed to provide very high voltage gain, and being built around a boost topology it's natural operation range for better utilization resides around 75% duty cycle.

To address this issue and share the current stress of the first stage, the setup of Fig. 1 is presented. In this case, the main converter inductor L_1, is supported by an additional inductor L_2, operated in parallel and in an interleaved manner to L_1. Inductor L_2, is not an equal member of the converter, but rather assists L_1 in charging the Boost capacitor C_1. L_2 is connected in a way that prevents it from interacting with other converter components to avoid forming an undesired current path at higher duty cycles. Despite the supportive nature of L_2, this setup enables to employ an interleaved operation between L_1 and L_2, sharing input current (I_{in}) and output current to C_1, resulting in reduced current ripple across both the input and C_1 capacitors. Primary inductor L_1 maintains the full system operation, providing current to C_1 via diode D_{a1} and to first stacked capacitor C_{S1}, L_2 provides the current to C_1 via the diode D_2, but it isn't connected to the first series stacked capacitor (C_{S1}).

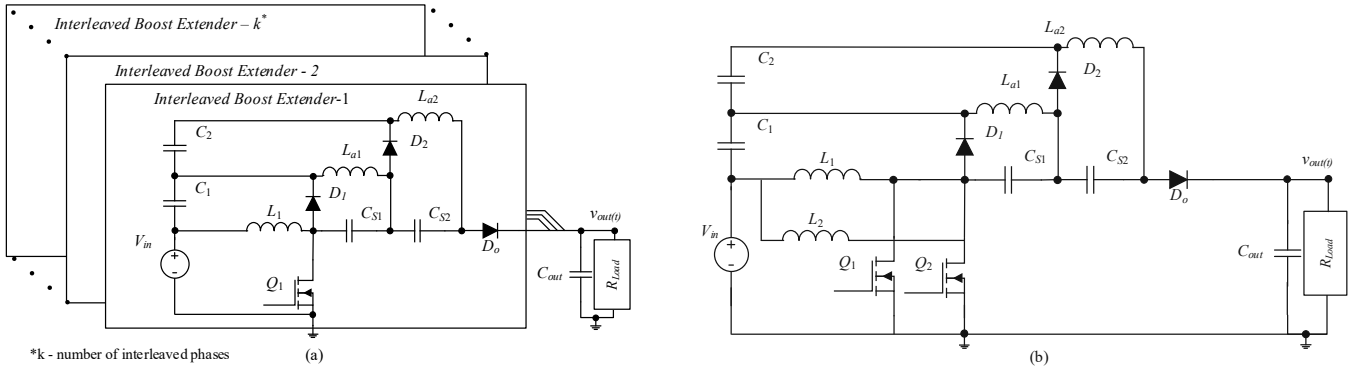

Figure 2: Potential interleaving schemes for boost extender: (a) Multiphase, (b) First stage interleaving (Switches Q_1 and Q_2 create unsuitable inductors short to the ground).

III. Interleaved Boost Extender Working Principle

For demonstration purpose, an interleaved Boost extender topology that includes one voltage extension module and two parallel interleaved stages is considered. Similar to boost extender converter topology this converter has two operation modes Continuous Conduction Mode (CCM) and Continuous Bidirectional Conduction Mode (CBCM). The operation mode is decided based on the auxiliary inductors L_{a1}, L_{a2}, ... L_{an} currents. When these currents are all time positive, converter operation is considered to be in CCM mode. If, however, the currents are changing direction, and become negative at least for part of the switching cycle, converter operation is considered to be in CBCM mode. Converter operation could be divided into 4-time intervals t_1, t_2, t_3 and t_4.

[t_1]: During this time interval the switch Q_1 and Q_2 are switched on and the diodes D_0, D_1 and D_2 are off Fig. 3(a). The primary inductor L_1 and supporting inductor L_2 currents are increased by the input voltage. The intermediate series capacitor C_{S1} is charged.

[t_2]: The switch Q_1 is on and the switch Q_2 is off, the diodes D_2 and D_0 are on, and diode D_1 is reverse biased. During this interval (Fig. 3b), V_{in} is applied to inductor L_1 and its current is increased, while L_2 provides energy to C_1 and to the load. Inductor L_{a1} transfers energy to the load. During this time interval C_1 is charging and C_{S1} is discharging.

[t_3]: During the third time interval (Fig. 3c), the switch Q_1 is off and Q_2 is on, diodes D_0, D_1 are forward biased and D_2 is reverse biased. L_1 current charges the auxiliary capacitor C_1 and supplies the load. Similar to t_2 interval C_1 is charging and C_{S1} is discharging.

[t_4]: During this time interval (Fig. 3d), the switch Q_1 and Q_2 both are off, and diodes D_0, D_1, D_2 are forward biased. Both primary inductor L_1 and supporting inductor L_2 provide energy to the auxiliary capacitor C_1 and the part of stored energy in L_{a1} supplies current to the load. The series capacitor C_{S1} discharges during this time interval.

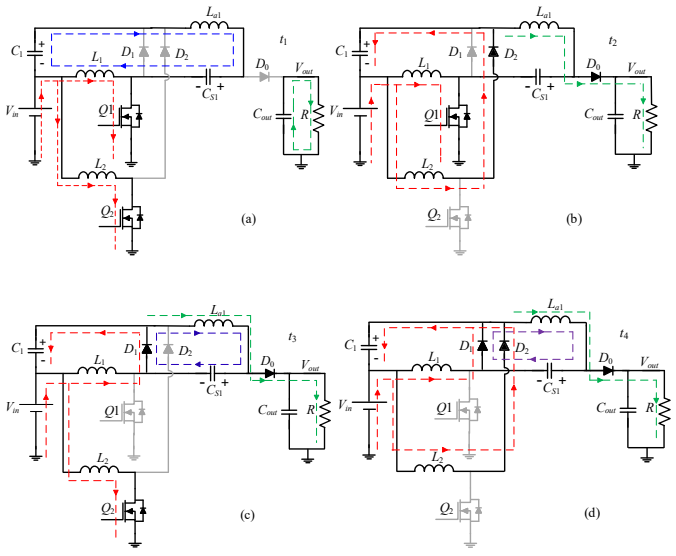

Figure 3: Operation phases by time interval: (a) t_1, (b) t_2, (c) t_3, (d) t_4.

IV. Simulation Results

In order to confirm the operation and features of the presented converter a simulation is performed in PSIM software by considering two interleaved stages, and two voltage extension modules of the converter (Fig. 1), with the following specifications: V_{in} = 15V, f = 100kHz, P_{out}=100W, Duty cycle (D) = 0.75, L_1 = L_2 = 100µH (Interleaved), L_1 = 200µH (Non-Interleaved) and L_{a1} = L_{a2} = 150µH.

Non-interleaved, single stage case waveforms are shown in Fig. 4a, and interleaved case is shown in Fig. 4b. The converter is operating in Continuous Bidirectional Conduction Mode (CBCM), where the energy from the auxiliary inductor L_{a1} is flowing in two directions, to the left, and to the right of the inductor. This happens when the inductor current I_{La1} crosses the zero axis, spending some time in the positive quadrant, and sometime in the negative quadrant of the axis (Fig. 5a). Similarly, CCM mode of operation is presented in Fig. 5b, where the energy of the auxiliary inductor L_{a1}, flows in a single direction, and the current, I_{La1} is always positive.

The Primary interleaved inductor currents I_{L1} and I_{L2} are 180^0 out of phase as shown in Fig. 5a,b. The ripple across the first auxiliary and series capacitors are shown in (Fig. 4a,b). Current ripple amplitude through C_1 for non-interleaved case is 6.58A while for interleaved operation mode it is reduced to 4.03A. Current ripple amplitude through C_{s1} is 8.74A and 6.41A respectively as shown in Fig. 4b,c. As expected from theoretical derivations, interleaved assistance stage for the main boost inductor reduces the current ripple through the first stacked auxiliary capacitor (Fig. 4a). In this case the ripple reduction is on the order of 39%. For the case of the first series capacitor (Fig. 4b) a current ripple reduction on the order of 25% has been demonstrated.

The nature of interleaving demonstrated in this work (Fig. 1), isn't classical, where both interleaving stages are equally sharing the full stress and operation phases of the circuit. In this case the second stage, is deemed as a supporting stage, and as such it doesn't directly shares the full burden of the input current with the main stage. This is shown in simulation results of (Fig. 5a,b). This happens because the switch node of the primary interleaved switch-inductor cell is not connected to the first series capacitor C_{s1}. The switch node of boost switch-inductor cell is connected to the series capacitor C_{s1}. The connection of the second stage, the interleaved switch-inductor cell with series capacitor C_{s1} can create undesired current path, due to both inductors connected to two switches operated with phase shift, which is unsuitable for the converter operation. To maintain proper converter operation and to avoid extreme current loops the supporting stage is disconnected from the series capacitor C_{s1}, and transfers charge only to the first, boost capacitor C_1, through its own diode D_m (Fig. 1). Partial participation in converter operation will create current imbalance between the first, the main stage, and the interleaved, supporting stage (Fig. 5b). To overcome the imbalance between the main boost inductor and the supporting interleaved inductor, duty cycle adjustments could be made to increase the supporting inductor current, and to equalize the two currents. Duty cycle adjustment to equalize the currents is demonstrated in Fig. 6. The duty cycle of the first stage is D_1 = 73%, and the duty cycle of the supporting stage was increased to be D_2 = 82% to equalize the two average currents to 1.25A.

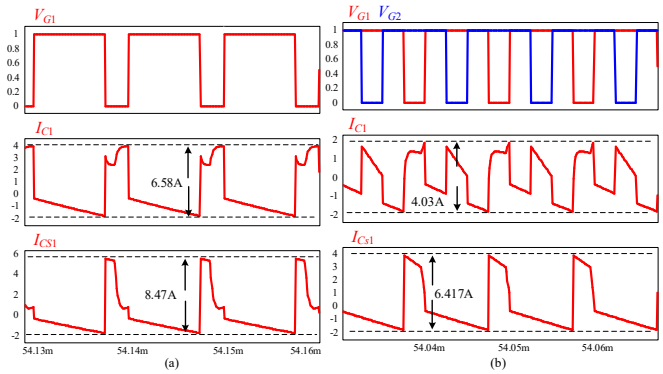

Figure 4: Gate signal V_{gs1}, V_{gs2} and (a) Capacitor Current Stress (I_{C1}, I_{CS1}) for non-interleaved boost extender, (b) Capacitor Current Stress (I_{C1}, I_{CS1}) for interleaved case.

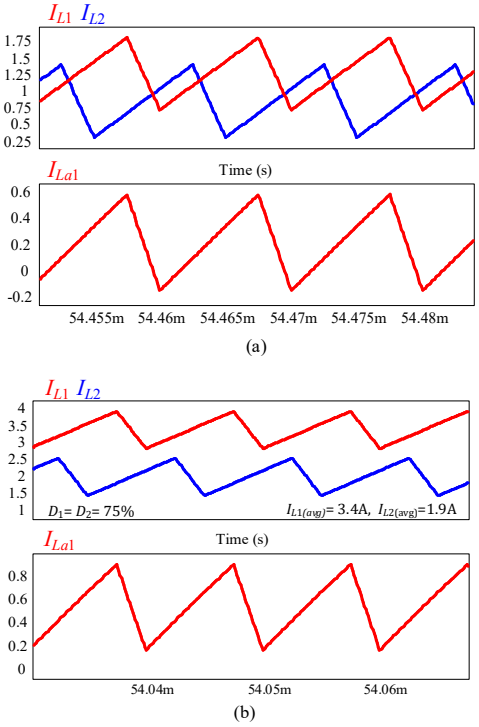

Figure 5: Interleaved Inductor Currents (I_{L1}, I_{L2}, I_{La1}): (a) CBCM mode of operation, (b) CCM mode.

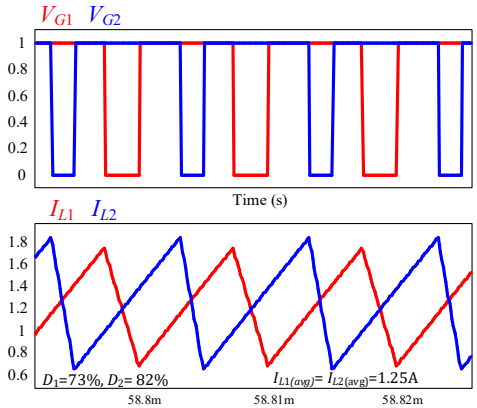

Figure 6: Gate Signal (V_{G1}, V_{G2}), Primary Interleaved Inductor Currents (I_{L1}, I_{L2}).

V. Experimental Results

To validate the topology operation, a 260W hardware experimental laboratory prototype with two interleaved stages, and two voltage extension modules has been built and evaluated. The converter was controlled using a MICROCHIP dsPIC33FJ16GS microcontroller. The specifications of the experimental prototype are shown in Table I.

TABLE I: Experimental Parameters

Input voltage V_{in}	15 V
Output voltage V_o	150 V
Maximum Output Power P_o	260W
Switching Frequency f	100KHz
Primary Inductors L_1	100 µH,400mΩ
Primary Inductors L_2	100 µH, 400mΩ
Inductors L_2, L_3	150 µH, 150 µH, (215mΩ)
Capacitors C_{s1}, C_{S2}	20 µF, 20 µF
Capacitors C_1, C_2	15 µF, 15 µF
Diodes	V40PW22CHM3/I
Main Switch	IXFH120N30X3
Microcontroller	dsPIC33FJ16GS

A maximum efficiency of 94% is achieved at 150W. The key waveforms are presented in Fig. 8-10 by considering V_{in} = 15V and P_o = 100W. For non-interleaved converter, the primary inductance was selected to be L_1 = 200µH, and for fair comparison interleaved converter primary inductors L_1 and L_2 were selected to be 100µH each. The primary inductor (I_{L1}, I_{L2}) currents are shown in Fig. 8a, while Fig. 8b shows the currents of the auxiliary inductors (I_{La1}, I_{La2}) where both currents crossing the zero axis which sets the converter operation to CBCM mode. The converter is operating with a 75% duty ratio, which is identical for both gate signals (V_{gs1}, V_{gs2}). Both signals are phase shifted by 180^0 as shown in Fig. 8a,b. Input (I_{in}) and first auxiliary capacitor ripple currents (I_{C1}) are shown in Fig. 9 and Fig. 10, where the ripples are significantly lower in interleaved boost extender case then for the non-interleaved converter case. Based on the experimental waveforms, it has been confirmed that the input current ripple is reduced by 46%, and the current ripple through the first auxiliary capacitor is reduced by approximately 50%.

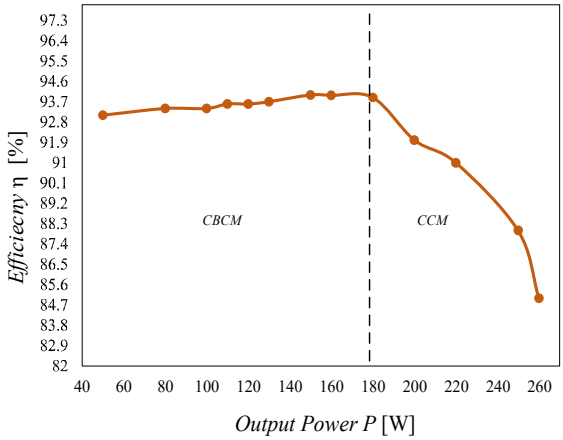

Figure 7: Efficiency curve for V_{in} = 15V, V_o = 150V.

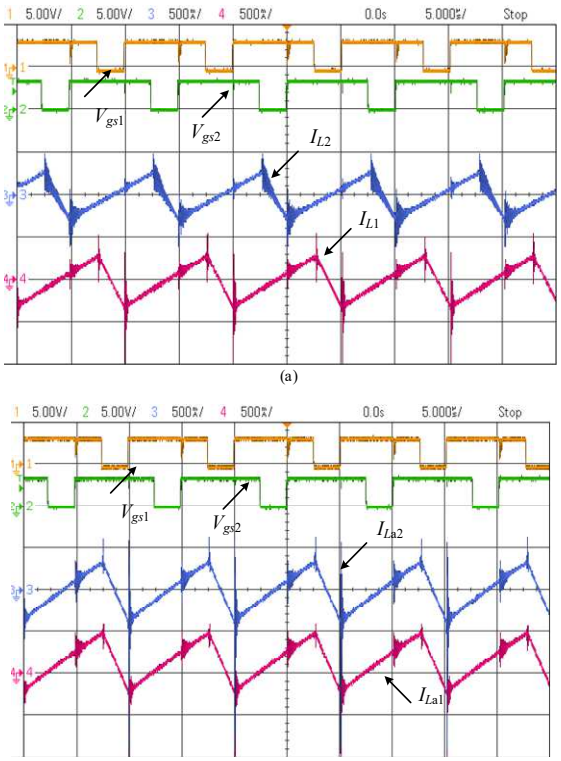

Figure 8: (Inductor currents), Gate signal $V_{gs1,}$ V_{gs2} and Inductor Currents (I_{L1}, I_{L2}, $I_{La1,}$ I_{La2}). Top trace is $V_{gs1,}$ V_{gs2} with 5V/Div, Bottom trace: (a) I_{L2}, I_{L1} with 500mA/Div, (b) $I_{La1,}$ I_{La2} with 500mA/Div, Time base is 5us/div.

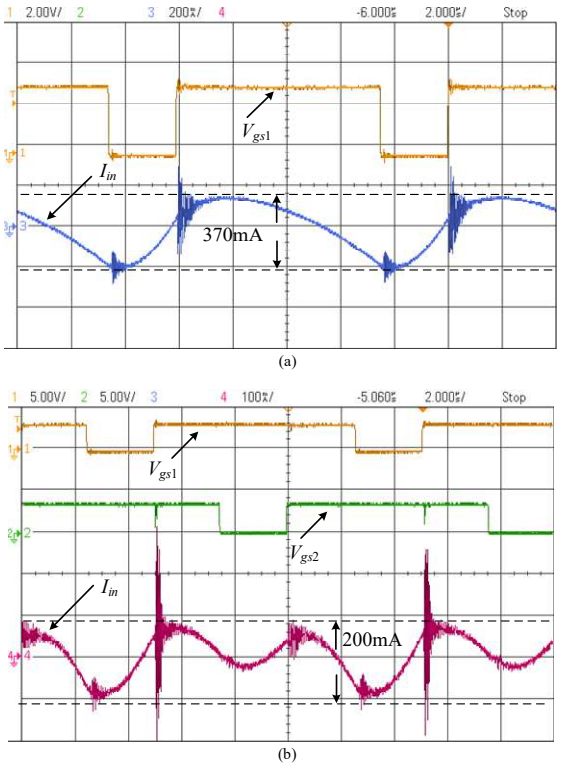

Figure 9: (Input current (I_{in}) ripple), Gate signal $V_{gs1,}$ V_{gs2} and Input Current (I_{in}). Top trace is $V_{gs1,}$ V_{gs2} with 5V/Div, Bottom trace:(I_{in}), (a) Non-Interleaved (I_{in}) with 200mA/Div, (b) Interleaved (I_{in}) with 100mA/Div, Time base is 2us/div.

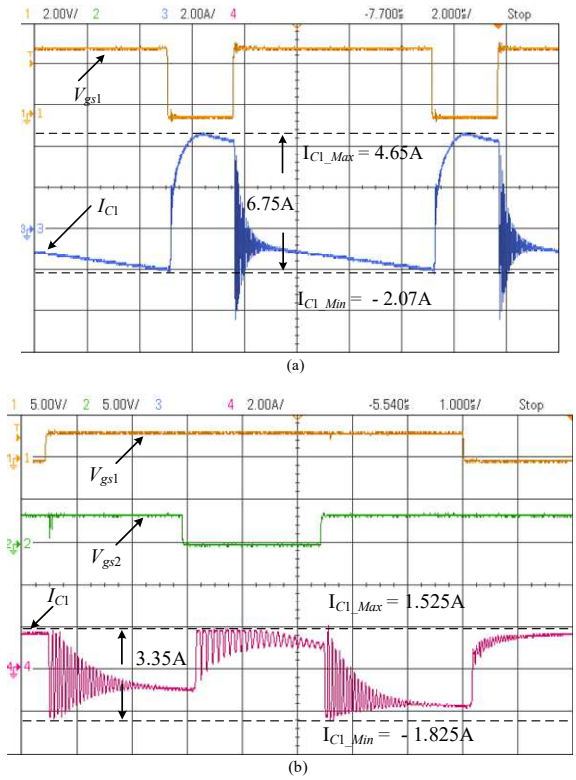

Figure 10: (Boost capacitor (I_{C1}) current ripple), Gate signal $V_{gs1,}$ V_{gs2} and Boost capacitor current (I_{C1}). Top trace is $V_{gs1,}$ V_{gs2} with 5V/Div, Bottom trace:(I_{C1}), (a) Non-Interleaved (I_{C1}) with 2A/Div, (b) Interleaved (I_{C1}) with 2A/Div, Time base is 1us/div.

The efficiency curve as a function of power level for input voltage of 15V and gain of 10 is presented in Fig. 7. The converter offers higher efficiency in CBCM operation mode compared to CCM mode ([15], [20]). At lower loads the converter operates in the CBCM operation mode. In this mode load increase results in minor efficiency increase due to the higher relative part of the average current transfer to the output, and constant losses relative part becomes smaller. Around 180W the converter switches from CBCM to CCM operation mode. This transition results in slightly lower efficiency as shown in Fig. 7. Lower efficiency in the CCM operation mode is a result of higher core losses, caused by higher currents through auxiliary inductors, and through the switch.

VI. CONCLUSION

An interleaving scheme for boost extender converter is presented. Three alternatives to interleaved operation and current stress reduction are discussed. A supporting parallel stage to share the current stress of the first stage is shown to assist in maintaining interleaving operation and capacitor current ripple reduction. Interleaving only the first stage out of the ladder of multiplication modules saves significantly on the component number comparing to traditional interleaving method. The concept was validated on a 260W experimental laboratory prototype achieving half the ripple in input and first stage output capacitors. Theoretical predictions well agree with simulation and experimental results.

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