Non-Isolated High Conversion Ratio Boost Extender Based on Back-end Series Capacitor Stacking

Vikas Kumar Rathore, *Student Member*, *IEEE,* Michael Evzelman,*Member*, *IEEE* and Mor Mordechai Peretz, *Member*, *IEEE*

The Center for Power Electronics and Mixed-Signal IC, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev, P.O. Box 653, Beer-Sheva, 8410501 Israel
rathore@post.bgu.ac.il, evzelman@bgu.ac.il ,morp@bgu.ac.il
http://www.ee.bgu.ac.il/~pemic

2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL) | 978-1-6654-1081-6/22/$31.00 ©2022 IEEE | DOI: 10.1109/COMPEL53829.2022.9829993

***Abstract* – A non-isolated high conversion ratio boost extending method is presented. The extender approach hinges on the stacking of series capacitors, to achieve high voltage gain, along with high efficiency. The series capacitor stacking method, facilitates a high efficiency single cycle energy conversion that eliminates the need in multiple consecutive conversions typical for high gain non-isolated converters. In addition, the topology and stacking approach features low voltage stress across the diodes and stacked capacitors. An analysis of the voltage gain and component stresses for the general case is carried out, and experimental prototype of 125W is developed and built in the laboratory. The converter attains maximum efficiency of 95.5% at input voltage of 20V and output voltage of 210V. The experimental results are in a good agreement with theoretical predictions.**

Keywords –Boost extender, Capacitor stacking, High voltage gain, Single-switch, Switched capacitor.

I. INTRODUCTION

During the last several years a number of single switch boost converter topologies have been proposed to achieve the high voltage gain ratio [1]-[4]. The conventional boost converter is a standard non-isolated step up converter and is widely used for the commercial and industrial applications. However, due to the parasitic losses, high current and voltage stress across the switches, boost converter doesn't provide a sufficient performance for very high voltage gain applications, and its efficiency at higher duty cycles is rather low [5]-[6]. To overcome the basic boost limitation a number of works applied a coupling inductor to increase the gain of a bare boost converter, and alleviate the limitation imposed by high duty cycle ([7]-[12]). The traditional coupled inductor based Boost converter such as Cuk or SEPIC converter [13] could be a good option to achieve high voltage gain conversion ratio, but due to the leakage inductance across the coupled inductor the main switch suffers from high voltage spike when switch is turned off, which results in high power loss. To overcome the losses a resistor-capacitor-diode (RCD) based snubber circuits are generally used to suppress the voltage spikes across the switch ([14]-[15]). So, many of lossless clamped circuit based boost topologies are recently proposed ([16]-[18]). An alternative approach using switched capacitor-based converters [19], has a potential to reach higher gains, but requires a large number of switches and isn't straightforward to achieve continuous regulation while maintaining an acceptable efficiency [20].

To further improve the voltage gain capability of non-isolated single switch converters and maintain high efficiency a different approach is needed. One option is a series capacitor buck converter, where a double voltage reduction is taking place in a single conversion ([21]-[22]). The unique methodology is in carrying out twice or more the voltage decrease, while paying with efficiency reduction only once. This is possible due to the converter structure, where an inductor from one substage, and a capacitor from a subsequent substage are charged/discharged serially in the same subcircuit, and during the same time frame. Moreover, the charging/discharging procedure is uniquely supported by both components, and as a result both the inductor and the capacitor contribute each to voltage reduction independently, while being part of a single charge/discharge process.

One more widely popular method to be mentioned is a resonant-inductive-boosting technique, as explored in [23]. In this case, a loosely coupled air-cored transformer is used to attain a very high voltage gain. One downside though with this topology is again a large leakage inductance loss, similar to the coupled inductor-based converters, which require an additional circuit to deal with the leakage inductance energy.

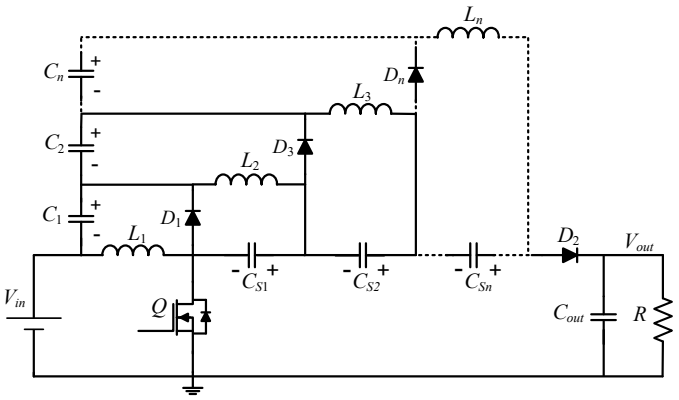


Figure 1: Boost extender high voltage gain converter topology.

Another point to consider is that these converters are bulky and complex due to the large air cored high frequency transformer, making it challenging to reach high voltage gain with high power density.

A novel generic approach of stacking multiple stages of series capacitor, to achieve single stage conversion for multiple voltage increase steps with no efficiency penalty is introduced in this study. The Boost extender topology with *n* fundamental cells stacked on top of each other is shown in Fig. 1. Each fundamental cell consists of an inductor, switched capacitor, auxiliary capacitor and a diode. In this article the stacked capacitors C_1, C_2, C_3 are referred as auxiliary capacitors, and the series capacitors C_{s1}, C_{s2}, C_{s3} are called switched capacitors. The rest of the article is organized as follows: Section II presents the working principle and the series capacitor stacking approach on a boost converter (Fig. 1), in section III a theoretical derivation of the voltage gain and components stress are carried out, section IV discussed the design guideline, section V explains simulation and experimental results and conclusions are drawn in section VI.

II. Working Principle

To demonstrate the working principle, Boost extender topology that includes three inductors is considered. The converter has two operation modes Continuous Conduction Mode (CCM) and Continuous Bidirectional Conduction Mode (CBCM). The operation mode is decided based on the L_2 and L_3 currents. When these currents are all time positive, converter operation is considered to be in CCM mode. If, however, the currents are changing direction, and become negative at least for part of the switching cycle, converter operation is considered to be in CBCM mode. First a CCM mode is analysed, but the two operation stages and conduction loops are identical for both CCM and CBCM modes.

The first stage begins at t = 0 and is finished at t = DT. The switch S is turned ON at the beginning of this time period, enabling loops 1, 2 and 3 as shown in Fig 2a.

All the diodes D_1, D_2 and D_3 are reverse biased at this stage and don't conduct. The output is fed by the output capacitor. Primary inductor L_1 is being charged by the input voltage V_{in}, loop 1 and inductors L_2 and L_3 are being charged by V_{in}, C_1 and C_2 as shown in loop 2 and loop 3. Series capacitors C_{s1} and C_{s2} are charged by V_{in}, and also by the auxiliary capacitors C_1 and C_2 as shown in loops 2 and 3. At the end of the first stage the inductors and series capacitors are charged, while the auxiliary capacitors are discharged.

Second stage begins with the main switch S being turned OFF, as shown in Fig. 2b. The diodes D_1, D_2 and D_3 are all forward biased and begin to conduct, enabling the loops 5 – 9 (Fig. 2b). During this stage L_1 transfers the stored energy to auxiliary capacitor C_1, loop 6 and to the load, loop 5. Inductor L_2 transfers its energy to C_2 and the load, loops 7 and 8. Finally inductor L_3 is discharge to the load, loop 9. Series capacitors C_{s1} and C_{s2} are discharged in this state as shown in loop 5. At the end of this stage, the inductors and series capacitors are discharged to their low, while the auxiliary capacitors are charged to their maximum.

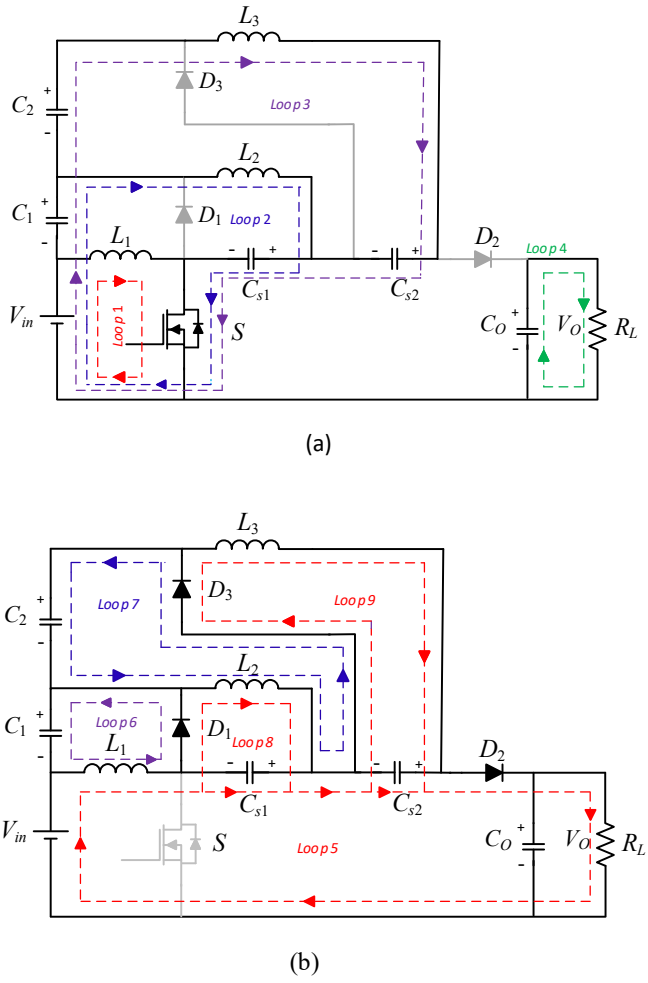


Figure 2: Boost extender high voltage gain topology

It should be noted here that during the first stage, series capacitors C_{s1} and C_{s2} are charged by V_{in} and auxiliary capacitors C_1 and C_2 via loop 2 and loop 3, which include inductors L_2 and L_3 in their charging path as shown in Fig. 2a. In the same way during the second stage, the auxiliary capacitors C_1 and C_2 have both inductors L_2 and L_3 in their charging path as shown in loop 6 and loop 7 in Fig. 2b. At no point in time the capacitors are connected to one another without an inductor in their path. This unique topology setup, ensures current source type charging of the capacitors, avoiding CV^2 losses, which reduces the capacitor charging loss, and allows the converter to achieve higher efficiency.

The working principle of proposed converter in CBCM is nearly the same as in CCM mode (Fig. 3), save the current through the auxiliary inductors L_2 and L_3, which flows in the negative direction for part of the cycle as shown in Fig. 3a. Due to the converter design, the main inductor L_1 is always in CCM mode, and as a result there is no DCM operation mode considered. However, as with the DCM operation mode CBCM is impacted by the load and the inductance. Higher load and larger inductor results in deeper CCM mode, and lower load and smaller inductance result in CBCM operation mode.

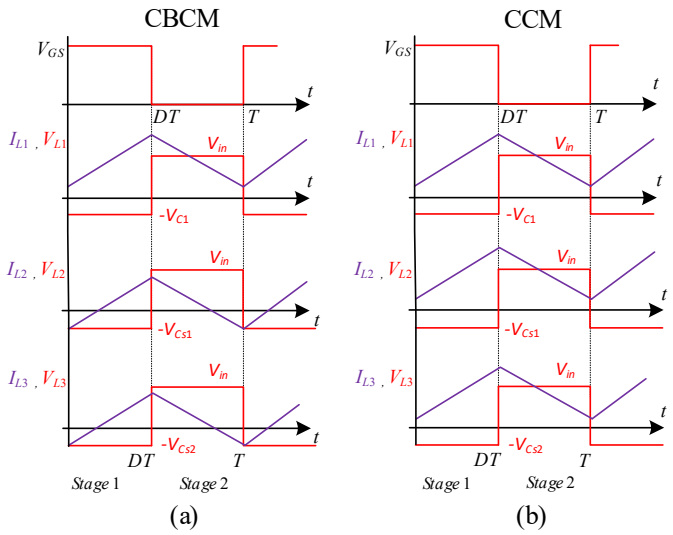


Figure 3: Inductor current waveform in one switching period

III. STEADY-STATE ANALYSIS

To analyse the converter in steady state operation we assume that all active and passive elements are ideal, input voltage V_{in} is constant, and all the capacitors are large enough so that the voltage ripple across them is negligible.

A. Voltage Gain

Applying the Volt-Second balance on the primary inductor L_1 (1), auxiliary inductor L_2 (2) and L_3 (3) the following equations have been obtained:

$$V_{in}.DT_s = V_{C1}.(1-D)T \quad (1)$$

$$(V_{in}+V_{C1}-V_{Cs1}).DT = V_{Cs1}.(1-D)T \quad (2)$$

$$(V_{in}+V_{C1}+V_{C2}-V_{Cs1}-V_{Cs2}).DT_s = V_{Cs2}.(1-D)T \quad (3)$$

Following the loops shown in Fig 2(b) we can apply the KVL on the fifth and sixth loops (4), and on the fifth and seventh loops (5).

$$V_{in}+V_{C1}+V_{Cs1}+V_{Cs2}=V_0 \quad (4)$$

$$V_{in}+V_{C1}+V_{C2}+V_{Cs2}=V_0 \quad (5)$$

By subtracting equation (4) from (5) we find that the first serial capacitor voltage is equal to the second auxiliary capacitor voltage.

$$V_{Cs1}=V_{C2} \quad (6)$$

Substituting this new equation (6) into (3) we reach:

$$V_{Cs2} = D(V_{in}+V_{C1}) \quad (7)$$

And now using (7) and substituting it into (1) we find that second serial capacitor voltage is equal to the first auxiliary capacitor.

$$V_{Cs2} = V_{C1} \quad (8)$$

Finally, from equations (1) and (2), equation (9) emerges.

$$V_{Cs1} = V_{C1} \quad (9)$$

Equations (6), (8) and (9) indicate that the voltages across all the series capacitors are equal to the voltages across all the auxiliary capacitors:

$$V_{C1}=V_{C2}=V_{Cs1}=V_{Cs2} \quad (10)$$

By the virtue of converter modularity, equation (10) is true for any number of modules in an ideal converter, and it means that any series capacitor and any auxiliary capacitors have the same voltage.

Using equation (10), and substituting equation (1) into (5), the voltage gain of the Boost extender converter presented here can be obtained:

$$\frac{V_o}{V_{in}}=\frac{(1+2D)}{(1-D)} \quad (11)$$

and the voltage gain for general case Boost extender converter can be written as:

$$\frac{V_o}{V_{in}}=\frac{(1+nD)}{(1-D)} \quad (12)$$

where n refers to the number of stacks or series capacitors we use for the converter. Voltage gain comparison of the presented two-stacked capacitor, conventional boost converter, and the converter shown in [7] is demonstrated in Fig. 4.

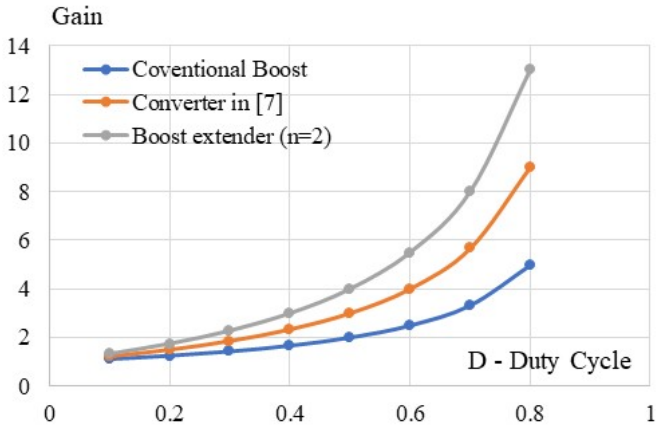


Figure 4: Voltage Gain vs Duty ratio

B. Voltage stresses

The unique feature of the topology presented here is that the voltage stresses across all the capacitors and the diodes are equal and using equation (1) and (10) can be expressed as:

$$V_{C1} = V_{C2} = V_{Cs1} = V_{Cs2} = V_{in}\frac{D}{1-D} \tag{13}$$

Applying KVL in loop 5 and 6 (Fig. 2b), the voltage stress across the switch can be obtain as in the conventional boost case:

$$V_{SW} = \frac{V_{in}}{1-D} \tag{14}$$

Examining loops 5, 6 and 7, the voltage stress across the diodes could be summarized as:

$$V_{D1} = V_{D2} = V_{D3} = \frac{V_{in}}{1-D} \tag{15}$$

From (14) and (15) it becomes clear that the voltage stress across the active and passive switching elements is limited to that of the conventional boost converter, while overall voltage gain is multiplied using the stacked capacitor approach. In addition, the voltage stress across the capacitors is even lower than the stress across the switches (13).

IV. Design Guide

Converter operation mode is majorly dictated by the passive components, inductors and capacitors. To assist in their selection, the basic relationships are derived below.

A. Design of Inductors L_1, L_2 ... L_n

To design the converter for operation in a CCM or CBCM mode a calculation of the borderline inductance value for CCM-CBCM limit is carried out. Using the inductor relation for a switching cycle, the expression for L_2 and L_3 is written as:

$$L_2 = \frac{(V_{in} + V_{C1} - V_{Cs1})}{0.2\Delta I_{L2}}DT \tag{16}$$

$$L_3 = \frac{(V_{in} + V_{C1} + V_{C2} - V_{Cs1} - V_{Cs2})}{0.2\Delta I_{L3}}DT \tag{17}$$

Applying (10) and due to the fact that the voltage across the auxiliary and switched capacitors are equal, (17) can be written as:

$$L_2 = L_3 = \frac{V_{in}DT}{0.2\Delta I_L} \tag{18}$$

Inductor value for general Boost extender case can be written as:

$$L_n = \frac{V_{in}DT}{0.2\Delta I_L} \tag{19}$$

B. Design of Capacitors C_1, C_2, C_{s1}, C_{s2} and C_o –

The value of capacitance is calculated by following expression:

$$C_1 \geq \frac{\left(\frac{I_{D3}}{(1-D)} - I_{L3}\right) + \left(\frac{I_{D1}}{(1-D)} - I_{L2}\right)}{\Delta V_{C1}}DT \tag{20}$$

$$C_2 \geq \frac{\left(\frac{I_{D3}}{(1-D)} - I_{L3}\right)}{\Delta V_{C2}}DT \tag{21}$$

For calculating the value of series stacked capacitors. We have assumed that during the steady state condition that the average current of the inductors I_{L1} and I_{L2} is equal to load current I_o.

$$C_{s1} \geq \frac{\left(\frac{I_{D3}}{(1-D)} - I_{L2}\right)}{\Delta V_{Cs1}}DT \tag{22}$$

$$C_{s2} \geq \frac{\left(\frac{I_{D2}}{(1-D)} - I_{L3}\right)}{\Delta V_{Cs2}}DT \tag{23}$$

$$C_o \geq \frac{\left(\frac{I_{D2}}{(1-D)} - I_o\right)}{\Delta V_{Co}}DT \tag{24}$$

V. Simulation and Experimental Results

A. Simulation Results

The designed boost converter topology with two stacked series and auxiliary capacitors is modelled in the PSIM simulation software in order to verify operation and the key wave forms. The simulation parameters are V_i=20V, D=0.75, fs=100kHz, V_o= 199V and voltage gain of 10 is used while performing simulation. The primary inductor L_1 value 100µH, auxiliary inductors L_2, L_3 =150µH, switched capacitor C_{s1}, =C_{s2} =11.4 µF and auxiliary capacitors of value C_1 =22.4 µF, C_2 = 11.4 µF is considered for the obtaining the waveforms in both CCM and CBCM mode.

Nominal load is used to verify converter operation in CCM as shown in Fig. 5a. A lighter load is used to demonstrate converter operation in CBCM mode as presented in Fig. 5b. inductor's L_1, L_2 and L_3 current waveforms are shown relative to the gate drive signal of the main switch.

B. Experimental Results

To validate the topology and the theoretical derivations presented in this study, a laboratory experimental prototype

with two back-end stacked series capacitor was built and evaluated as shown in Fig. 8. A 125W hardware prototype has been developed and tested in laboratory. The specifications of the experimental prototype are shown in Table I. A maximum efficiency of 95.5% is achieved, when it is operated in the CBCM mode with the load value of 500 ohm, which are 70% of the nominal load.

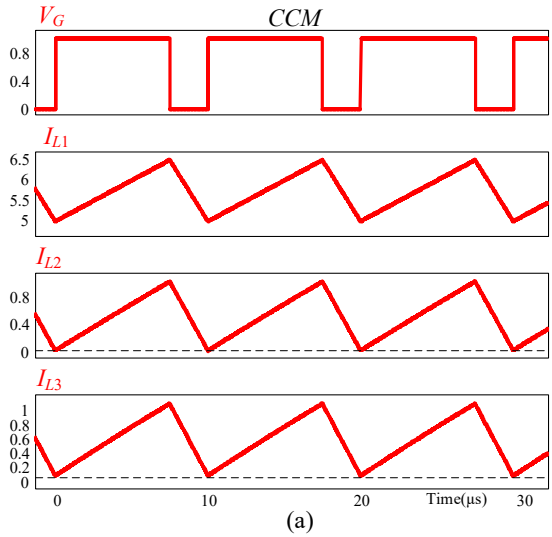


Figure 5: PSIM software simulation waveforms in (a) CCM, (b) CBCM.

TABLE I : EXPERIMENTAL PARAMETERS

Input voltage V_{in}	20 V
Output voltage V_o	210 V
Output Power P_o	125W
Switching Frequency f_o	100KHz
Primary Inductors L_1	100 μH
Inductors L_2, L_3	150 μH, 150 μH
Capacitors C_{s1}, C_{S2}	20 μF, 20 μF
Capacitors C_1, C_2	15 μF, 15 μF
Diodes	V40PW22CHM3/I
Main Switch	IXFH120N30X3

The voltage stress across the switches is measured as $V_S = V_{D1} = V_{D2} = V_{D3} = 79.25$V and across the capacitors as $V_{c1} = V_{c2} = V_{cs1} = V_{cs2} = 59.89$V. Voltage stresses are in a good agreement with the theoretical predictions. In Fig 5 the theoretical and experimental gains of the converter are verified by varying the duty ratio. Experimental measurements of the voltage gain are tightly following the theoretical analysis and simulation results as shown in Fig. 6.

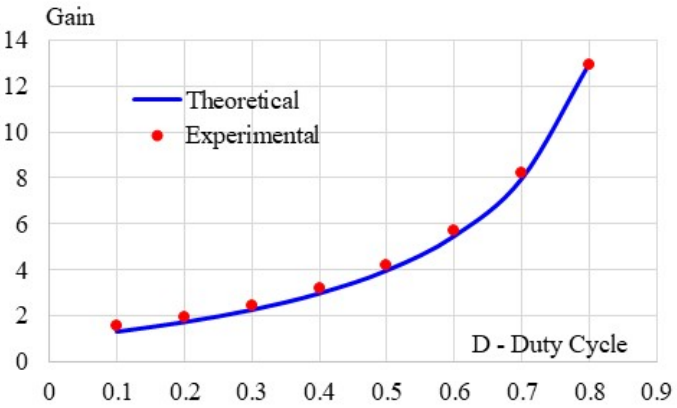


Figure 6: Experimental and theoretical gain of Boost extender converter.

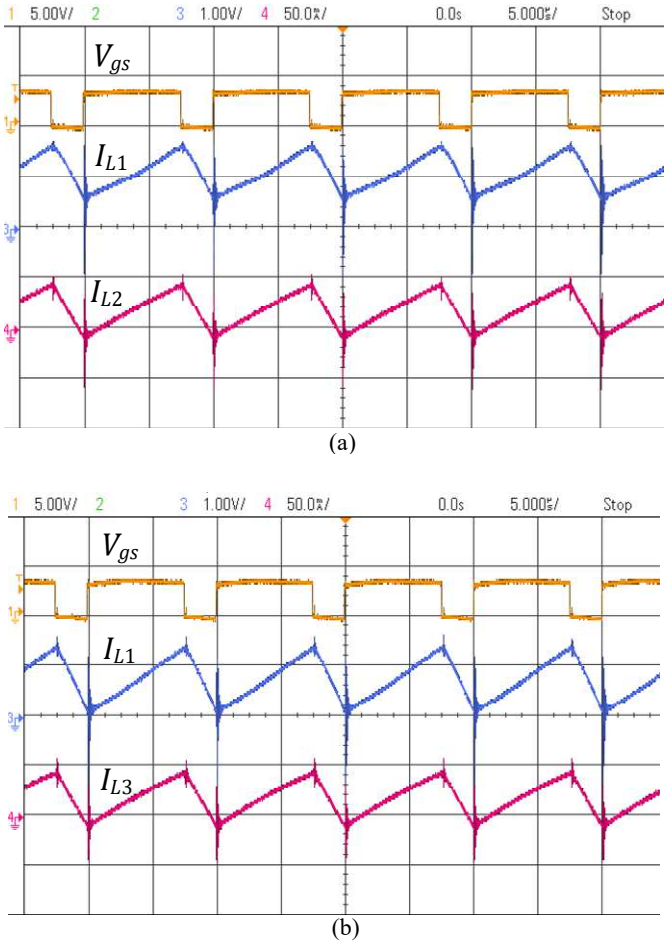
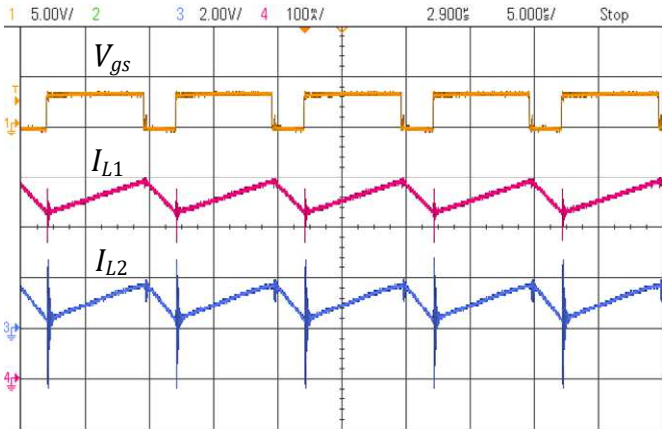
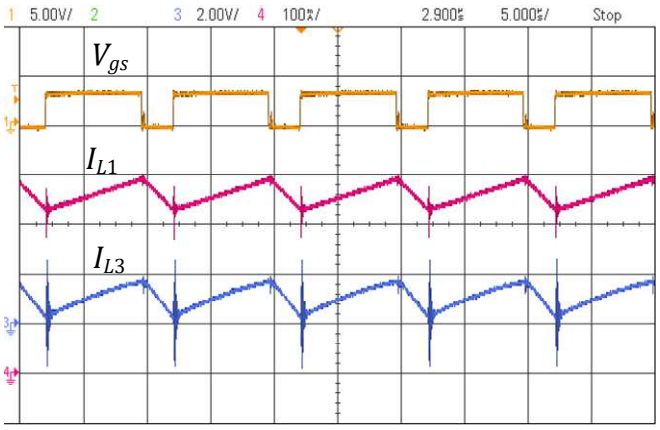


Figure 7: Experimental waveform in CBCM when P_0=100.63W, η= 95.5% and V_{in}=20V; Gate signal V_{gs} and Inductor Currents (I_{L1}, I_{L2}, I_{L3}). Top trace is V_{gs} with 5V/div; Middle trace is the I_{L1} with 1A/div; Bottom trace: (a) I_{L2}, (b) I_{L3} with 50 mA/div, Time base is 5us/div.

The operation of the converter in the CBCM mode is demonstrated in Fig. 7. The duty cycle signal is at the top, and the inductor current I_{L1} is in the middle. The bottom trace in Fig. 7a shows the I_{L2} current, and in Fig. 7b the I_{L3} current. While the primary current I_{L1} is fully above zero, in CBCM mode the currents I_{L2} and I_{L3} are going into the negative region for some time of the operation.



(a)



(b)

Figure 9: Experimental waveform in CCM when P_0=117.5W, η= 94% and V_{in}=17V; Gate signal V_{gs} and Inductor Currents (I_{L1}, I_{L2}, I_{L3}). Top trace is V_{gs} with 5V/div; Middle trace is the I_{L1} with 100mA/div; Bottom trace: (a) I_{L2}, (b) I_{L3} with 2 mA/div., Time base is 5us/div.

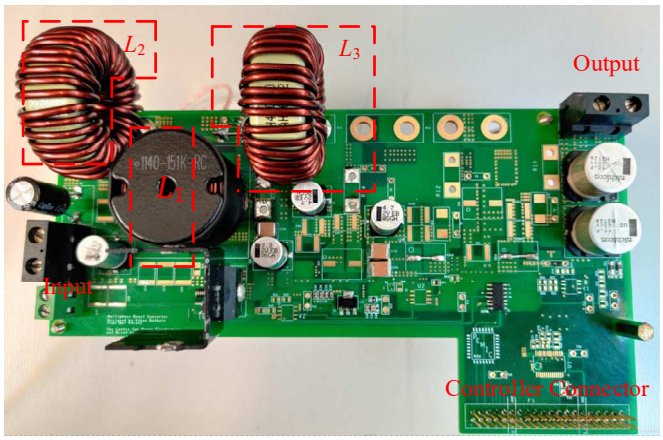


Figure 8: A photo of experimental prototype.

High Load value is considered for operating the converter in CCM mode. During the CCM mode the prototype has an output of 117.5W, with input voltage of 17V, running at 94% efficiency. Inductor current waveforms in CCM are shown in Fig. 9. The inductor current I_{L1} is in the middle, and the duty cycle signal is plotted at the top. The bottom traces in Fig. 9a are I_{L1} and I_{L2}, and in Fig. 9b bottom traces are I_{L1} and I_{L3}. In CCM mode all of the inductor currents are operating in the positive region. It can be seen from waveforms that the I_{L2} and I_{L3} are continuous and positive at all time.

VI. Conclusion

A Boost extender non-isolated single switch high voltage gain converter is presented in this article. A Boost extender structure enables to add as many back-end series capacitor stacking as required to increase the voltage gain. The unique stacking mechanism enables an efficient one cycle conversion, along with ensuring highly efficient charge transfer between the capacitors, where each transfer path includes an inductor to stir away from CV^2 losses. The voltage stress across the capacitors, diodes and switch is found to be equal or lower than in a conventional boost converter, while providing much higher voltage gain. Voltage gain and component stresses of the topology were derived.

A Boost extender experimental prototype of 125W having voltage gain of 10.5 is developed, built and evaluated in the laboratory. The experimental prototype attains maximum efficiency of 95.5% in CBCM mode at input voltage of 20V and output voltage of 210V. Slightly lower efficiencies were obtained in CCM mode. This is due to the higher rms current through the switch and inductors, which causes higher conduction losses. The experimental results were found to be in a good agreement with the theoretical predictions.

Acknowledgment

This research was supported by the ISRAEL SCIENCE FOUNDATION grant number 2186/19.

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