Non-Isolated Parallel Balancing Converter for Serially Connected Batteries String

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***Abstract*- This paper introduces a new balancing topology for serially connected batteries string. The balancing operation provides fast convergence of the cells using a non-isolated parallel balancing approach with a low voltage bus that is used as an energy buffer. Balancing of the string is achieved through voltage equalization of the cells. The converter is operated in DCM and the current that flows between the cells and the bus is a function of their voltage difference. As a result, the quiescent power loss is minimal since no energy circulates in the system when the cells are balanced. Furthermore, no voltage or current sensors are required, making the implementation of the system simple and cost-effective. Theoretical analysis as well as design guidelines for the construction of the new topology are detailed and then validated on an experimental prototype that demonstrates the balancing capability of the system.**

I. INTRODUCTION

Batteries have been widely used in various applications as an energy storage element and a power source. Due to limited cell voltage, to achieve the high voltage and high power required in applications such as electric vehicle (EV) and its derivatives, large number of batteries cells are connected in series [1]-[5]. Batteries suffer from degradation with aging, manufacturing and environmental variances, charging and discharging, thermal conditions, and internal impedance imbalance. Each of these potential flaws or a combination of them may lead to imbalances in the stored energy of the batteries and as a result reduce their lifetime, reliability and efficiency [6]. Therefore, strings of serially connected batteries must be assisted by a balancing circuit to minimize imbalances and improve the overall performance [7], [8].

In the majority of commercial battery balancing applications, primarily due to cost and simplicity, the passive balancing approach is predominant [9]. There, the excess energy of each cell is dissipated either through a resistor or transistor. From an energy efficiency perspective it is a lossy process and therefore less attractive. An alternative concept, that has been widely investigated in recent years, is the active balancing [10]-[27]. In this approach, power converters are employed to evenly distribute the energy along the series string. Typically, energy is transferred from cells of higher voltage to the lower ones, or in more sophisticated designs by balancing cell's State-of-Charge (SoC) [28], [29]. Active balancing can be realized in a variety of ways for example using switched-capacitors converters [10]-[12], switched inductor converters [13]-[24], or multi-winding transformer based converters [25]-[27].

Another important classification of balancing circuits is in the power flow architecture, i.e., series balancing and parallel balancing. In series balancing, e.g. as in [11], energy is transferred from one neighboring cell to another using a power converter that links between two adjacent cells and acts as a local bypass to the energy flow in case a cell is damaged or produces less energy. Parallel balancing is assisted by an energy storage component, typically a capacitor, and often referred as energy buffer which is used as a link to transfer energy from a charged cell to the cell that needs to be charged without the need to process the energy through the whole batteries string [30]-[32]. Therefore, an apparent advantage of the parallel balancing approach is the fewer amount of conversions to balance the string and as a result faster balancing with higher efficiency especially in large arrays. However, the penalty comes with the requirement of isolation which increases the complexity of the solution.

The objective of this study is to introduce a new non-isolated parallel batteries balancing topology with a simple sensorless implementation and reduced component count. The new topology, shown in Fig. 1, equalizes the voltage of all the cells to their average voltage using a common bus capacitor.

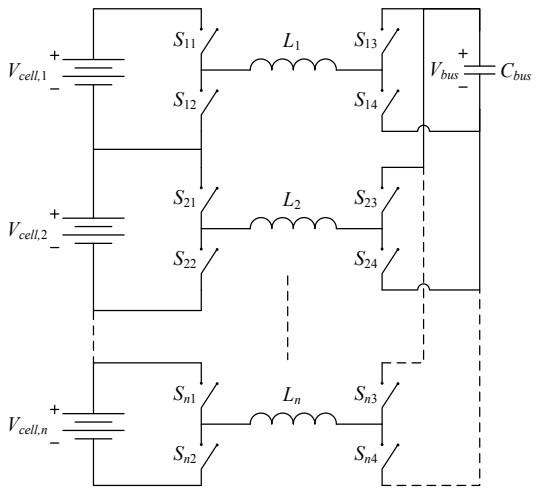

Fig. 1. Batteries balancing system for *n* serially connected batteries.

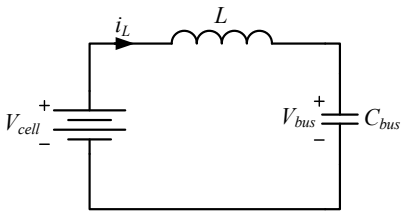

Fig. 2. Voltage equalizing mechanism of a battery cell and the bus capacitor.

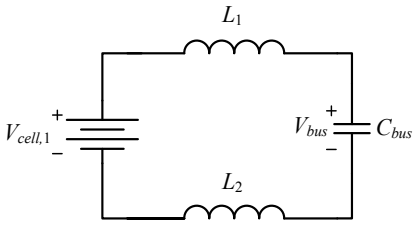

Fig. 3. The resultant circuit during on time when balancing $V_{\text{cell},1}$.

The overall volume and complexity of the system are reduced since neither transformers nor sensors are required. This is facilitated by utilizing conduction paths of a neighboring module to link with the energy buffer. Furthermore, an additional significant advantage of the new topology is that the quiescent power loss is minimal since no energy circulates in the system when the batteries are balanced.

The paper is organized as follows: Section II describes the topology, its principle of operation and the major features of it. Section III delineates the system's implementation and provides design guidelines. Experimental results are then provided in Sections IV, Section V concludes the paper.

II. Principle of Operation

The operation of the balancing system in Fig. 1 is based on voltage equalization between the batteries and the bus capacitor. By connecting a cell to the bus capacitor through an inductor, as shown in Fig. 2, the inductor current direction is governed by the polarity of the voltage difference and the current naturally flows toward to the source with the lower voltage and charges it.

In the system shown in Fig. 1, the bus capacitor is common for all the n batteries cells using n balancing modules, each consists of 4 switches and an inductor. The modules are bidirectional converters that operate sequentially, i.e. every switching cycle a different module is active. This procedure is repeated for all the batteries cells. Assuming similar cells, this results in a bus capacitor voltage that converges to the average of the cells' voltages, given by:

$$V_{bus} = \frac{1}{n}\sum_{m=1}^{n} V_{cell,m} \tag{1}$$

where V_{bus} is the bus capacitor voltage and n is the number of cells in the string. Since the bus is common for the entire string, all cells' voltages eventually balance and their voltages converge to (1).

A core concept in the presented balancing topology is to use the adjacent balancing module for a return conduction path to the current when balancing a certain cell. As a result, fewer switches are required and the inductor per module is of lower volume. For example, as can be seen in Fig. 3, when balancing $V_{\text{cell},1}$, the inductor L_2 of the adjacent module is used in the return path of the current. The system operation is set to DCM, so that the inductors' current at the beginning of the switching cycle is zero. This guarantees there is no current imbalance between the inductors. The direction of the current flow is

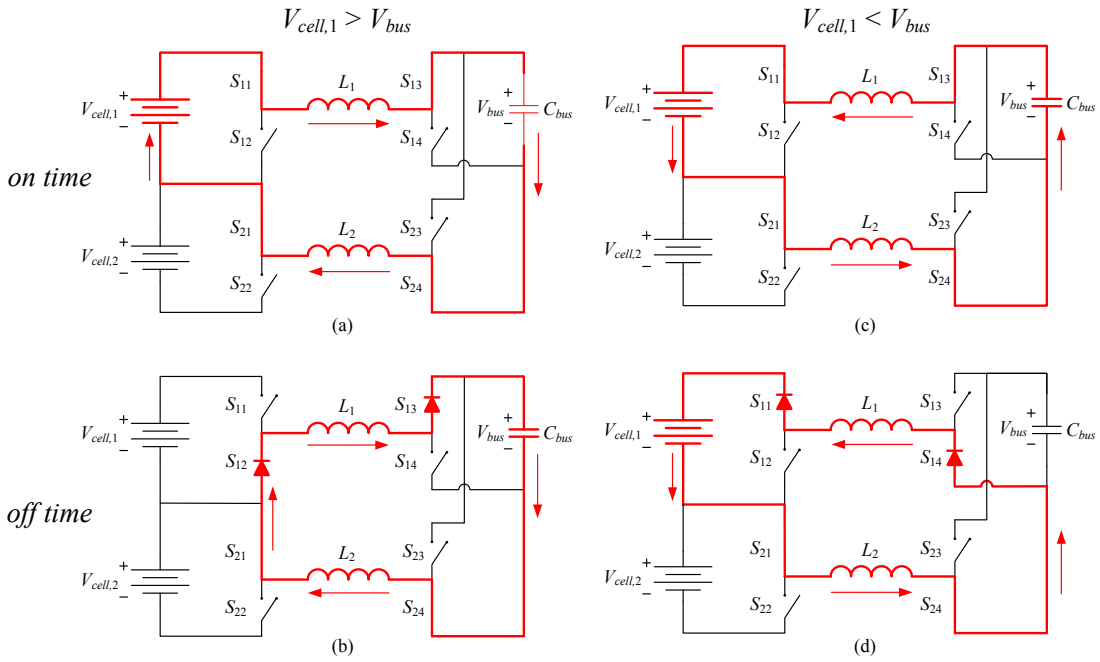

Fig. 4. Balancing operation of cell no. 1 for the case where $V_{\text{cell},1} > V_{\text{bus}}$: (a) on time, (b) off time, and for the case where $V_{\text{cell},1} < V_{\text{bus}}$: (c) on time, (d) off time. Arrows mark the current direction.

governed by the voltage difference between V_{bus} and V_{cell}, eliminating the need for current sensing. In the case that the voltages are equal, no current circulates through the circuit.

The balancing operation of cell no. 1 is demonstrated in Fig. 4. During the balancing period of the cell, the adjacent module's switches S_{21} and S_{24} are turned on to create a return path for the current. In the first step, switches S_{11} and S_{13} are on and the current in the inductors L_1 and L_2 ramps up or down, determined by the voltage difference polarity of $\Delta V=V_{cell,1}-V_{bus}$. In the case when $V_{cell,1} > V_{bus}$ (Fig. 4(a)) the energy is transferred from cell no. 1 to the bus capacitor, and in the case when $V_{cell,1} < V_{bus}$ (Fig. 4(c)) the energy is transferred in the opposite direction. In the second step, after the predefined on time that ensures operation in DCM (will be detailed in the following section) and regardless of the current direction, switches S_{11} and S_{13} are turned off. At this point, due to continuity of the inductors current, either the body diodes of switches S_{12}, S_{13} or S_{11}, S_{14} are forward biased for the case $V_{cell,1}>V_{bus}$ (Fig. 4(b)) or $V_{cell,1}<V_{bus}$ (Fig. 4(d)), respectively. The applied voltage on the inductors when the body diodes conduct is the minimum between $V_{cell,1}$ and V_{bus}, ramping down the current back to zero. The current remains zero until the start of the next switching cycle.

Fig. 5 shows the current and voltage waveforms for the case that $V_{cell,1}>V_{bus}$. During the on time, the inductors current ramps up with a slew rate of

$$\frac{di_L}{dt}=\frac{V_{cell,1}-V_{bus}}{L_1+L_2}. \tag{2}$$

During the off time, the applied voltage on the inductors is the minimum between the two voltages, and therefore the inductors current ramps down with a slew rate of

$$\frac{di_L}{dt}=-\frac{\min\left(V_{cell,1},V_{bus}\right)}{L_1+L_2}. \tag{3}$$

The body diodes stop conducting at the point where the current is zero. Neglecting the parasitic oscillations that are common for any DCM operation, the current remains zero until the next switching cycle.

The balancing of the adjacent cell no. 2 is shown in Fig. 6. In a similar manner to the balancing operation of cell no. 1, cell no. 2 is assisted by cell no. 1 for a current conduction path by turning on switches S_{13} and S_{12} during the balancing period of cell no. 2. In the first step, switches S_{22} and S_{24} are turned on and the inductors current direction is determined by the voltage difference $V_{cell,2}$ - V_{bus} (Fig. 6(a) and (c)). After a predefined on time switches S_{22} and S_{24} are turned off and the body diodes conduct: body diodes of S_{21} and S_{24} for $V_{cell2} > V_{bus}$ (Fig. 6(b)) and body diodes of S_{22} and S_{23} for $V_{cell,2} < V_{bus}$ (Fig. 6(d)).

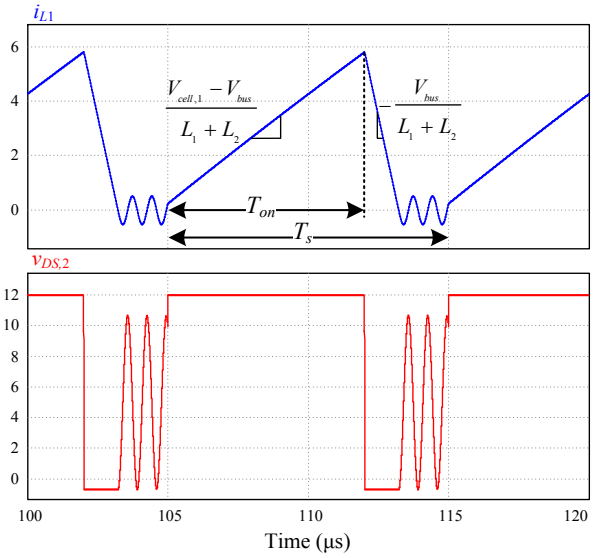

Fig. 5. Waveforms of the current in L_1 and voltage across switch S_{12} when balancing cell no. 1 for the case that $V_{cell,1} > V_{bus}$.

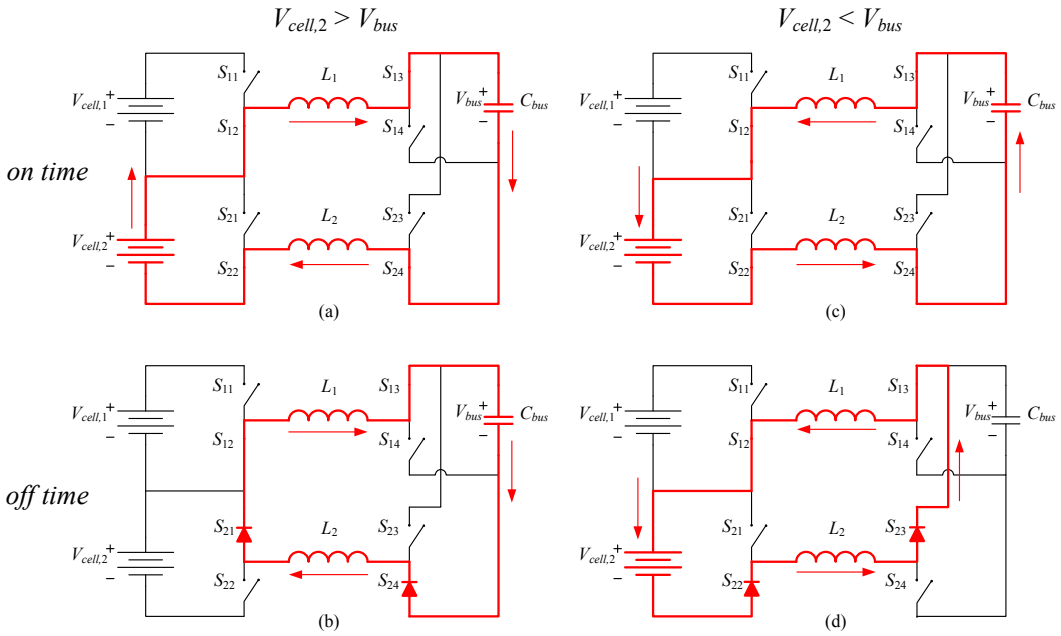

Fig. 6. Balancing operation of cell no. 2 for the case that $V_{cell,2} > V_{bus}$: (a) on time, (b) off time, and for the case that $V_{cell,2} < V_{bus}$: (c) on time, (d) off time.

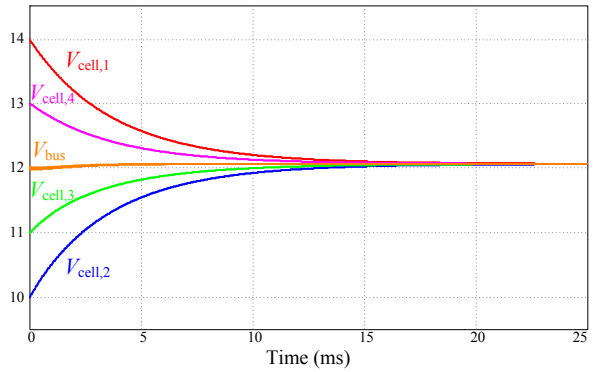

Fig. 7. Simulation results for 4 batteries cells emulated by large capacitors.

To demonstrate the balancing operation of the system, a simulation case study has been carried out and the results are shown in Fig. 7. It depicts the convergence of four cells (emulated by large capacitances), each set with different initial voltages, to the cells' average voltage, validating the balancing capability of the system.

III. Implementation and Design Considerations

To realize a cost-effective balancing system for the architecture described in Fig. 1, several practical design challenges need to be addressed. They include the power transistors configuration and the gate drivers, selection of the inductors and the resulting balancing current to satisfy DCM, and selection of the bus capacitor.

A. Bidirectional Switches and Gate Drivers Implementation

The use of a non-isolated topology forces the balancing modules to operate sequentially. This is done to avoid undesired current loops that may occur as a result of two distant modules that are operated at the same time. In addition, to eliminate additional current loops through the body diodes of the switches in the non-active modules when other modules are active, the switches on the bus side are realized as four-quadrant devices, constructed using two MOSFETs connected back-to-back, as depicted in Fig. 8.

The use of bidirectional switches presents an additional challenge related to the sensorless operation of the topology. As described in Section II, the body diodes of the switches conduct due to the continuity of the inductors current, and the specific body diodes that are forward biased depend on the current direction (see S_{13} in Fig. 4(b) and S_{14} in Fig. 4(d)). Therefore, to still benefit from the natural diode conduction, the bidirectional switches need to operate as diodes during the off time of the balancing operation. This rules out the possibility of driving them with the same gate signal and each should have its own driver with respect to the proper source potential. In this study, such configuration is realized by a simple bootstrapped driver as shown in Fig. 9. In this configuration, the bootstrap capacitor is connected to the source of the upper MOSFET, and when the lower MOSFET is on, the capacitor is charged through two diodes: the bootstrap diode D_B and body diode of the upper MOSFET, as highlighted in Fig. 9. Similar arrangement is used for the switches S_{m3} and S_{m3a} (Fig. 8).

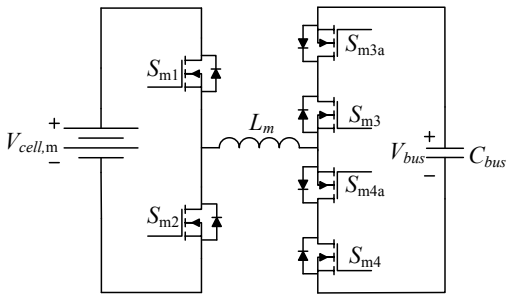

Fig. 8. Implementation of the switches for each balancing module with bidirectional switches using two MOSFETs.

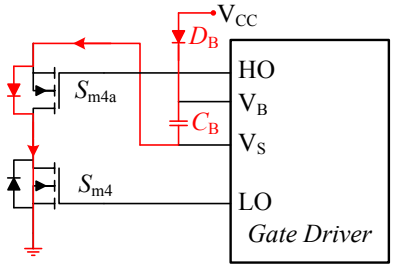

Fig. 9. Implementation of a bidirectional switch and an independent gate driver per transistor using a conventional bootstrapped driver. Bootstrap capacitor's current charging loop is marked in red.

B. Inductors, Bus Capacitor and Balancing Current Design

The main objective of the inductor in the module is to limit the balancing current as a result of two low-impedance sources (the cell and the bus capacitor) connect to each other. Therefore, the inductance value L, the on time of the switches T_{on}, and the voltage difference between the battery cell voltage and the bus capacitor voltage ΔV govern the current that flows through the inductor in every switching cycle. In the following analysis it is assumed that the inductors of all the balancing modules are equal with inductance L.

Since each balancing module operates in DCM, the peak inductor current I_{pk} and the inductors' current ripple ΔI_L are equal. As described earlier, the current flows through two inductors and therefore I_{pk} and ΔI_L are given by

$$I_{pk} = \Delta I_L = \frac{\Delta V}{2L} T_{on} . \tag{4}$$

After turning off the switches, the time it takes for the current to ramp down back to zero can be expressed as

$$T'_{off} = \frac{\Delta V}{\min\left(V_{cell}, V_{bus}\right)} T_{on} , \tag{5}$$

and the average inductors current in a single switching cycle is

$$I_L = \frac{\Delta V}{4L}\left(1 + \frac{\Delta V}{\min\left(V_{cell}, V_{bus}\right)}\right)\frac{T_{on}^2}{T_s} , \tag{6}$$

where T_s is the switching period.

As can be seen in (6), in the case that the cells are balanced and no voltage difference exists, i.e. ΔV=0, the inductors current is zero and no energy circulates through the system, resulting in a minimal quiescent power loss. To expedite the

convergence time, small inductance values may be selected. This is due to the higher current that can be delivered. However, it would require a design with lower stray resistance (switches and inductors) to avoid high conduction losses during balancing.

To guarantee the system's operation in DCM, T_{on} has to be limited. The maximum on time $T_{on,max}$ depends on the given maximum voltage difference ΔV_{max} and the minimum voltage between the battery and the bus, and it is given by

$$T_{on,\max} = \frac{\min\left(V_{cell}, V_{bus}\right)/\Delta V_{\max}}{1+\min\left(V_{cell}, V_{bus}\right)/\Delta V_{\max}} T_s \ , \qquad (7)$$

This implies that for a case where ΔV is expected to be high, the upper limit of T_{on} should be set sufficiently low to limit the peak current. However, the more practical case is where the string has relatively small voltage differences, i.e. ΔV is relatively low, in the range of tens of millivolts (in particular in Li-ion cells). In this case, the upper limit for the on time (along with the inductance value) would determine the total convergence time.

The capacitance of the bus capacitor that acts as an energy buffer between the cells should be sufficiently low with respect to the capacity of the batteries. This is to assure relatively fast convergence to the cells' voltages average value, as in (1). On the other hand, a small voltage ripple is desired at the bus voltage to minimize its effect on the balancing operation. Therefore, the minimum bus capacitance that should be used must satisfy the condition

$$V_{ripple} << \Delta V \ , \qquad (8)$$

where V_{ripple} is the voltage ripple of the bus capacitor. Using (6), (7) and after some manipulations, condition (8) translates into

$$C_{bus} >> \frac{T_{on,\max}^2}{4L} \ , \qquad (9)$$

where f_s is the switching frequency.

IV. Experimental Verification

In order to demonstrate the balancing operation and to verify the theoretical analysis and simulation results, several experiments have been carried out using two cells connected in series, emulated by large capacitors. Table I shows the components types and values of the experimental setup. The balancing time between the cells is shared equally, where one cell is being balanced for a switching cycle and the other is being balanced in the consecutive switching cycle.

Fig. 10 presents the steady-state operation current waveforms in L_1 and L_2 for unbalanced cells with T_{on}=0.5T_s. The measurements are taken when the cells' voltages are $V_{cell,1}$=8V and $V_{cell,2}$=12V and the bus voltage is V_{bus}=10V. Since the cells voltages are symmetrical with respect to the bus voltage (same voltage difference, but opposed polarity), the currents i_{L1} and i_{L2} are 180^0 out of phase and have the same magnitude.

Fig. 11 shows convergence of the cells' voltages when cell no. 1 is connected to a 12V DC power supply. As can be observed, when the convergence starts, the balancing system charges cell no. 2 and as a consequence $V_{cell,2}$ rises, while V_{bus}

TABLE I – Experimental Prototype Values

Component	*Value*
Batteries (emulated by large capacitors)	60 mF
Module inductors L_1, L_2	3.3 µH
MOSFETs S_{m1}-S_{m8}	30V, 5.7mΩ
Bus capacitor C_{bus}	100 µF
Balancing operation on time T_{on}	$1/2f_s$
Switching frequency f_s	100 kHz

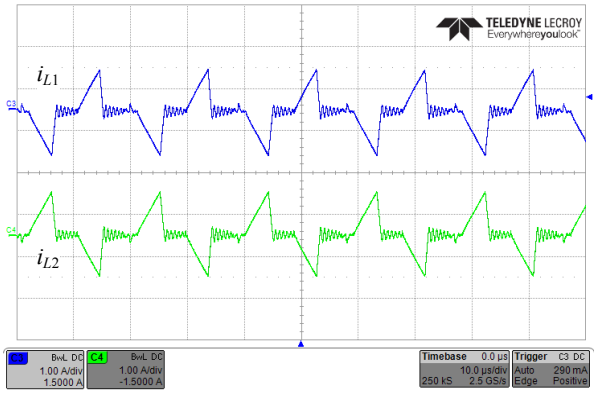

Fig. 10. Inductors currents for an unbalanced steady-state operation. C3 – i_{L1} (1A/div), C4 - i_{L2} (1A/div). Time scale is 10µs/div.

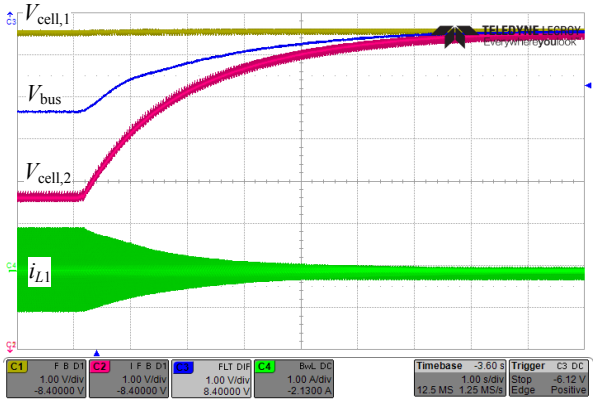

Fig. 11. Convergence of the cells' voltages when $V_{cell,1}$ is connected to a 12V DC power supply; $V_{cell,2}$ and V_{bus} converge toward $V_{cell,1}$. C1 – $V_{cell,1}$ (1V/div), C2 – $V_{cell,2}$ (1V/div), C3 - V_{bus} (1V/div), C4 – inductor current i_{L1} (1A/div). Time scale is 1s/div.

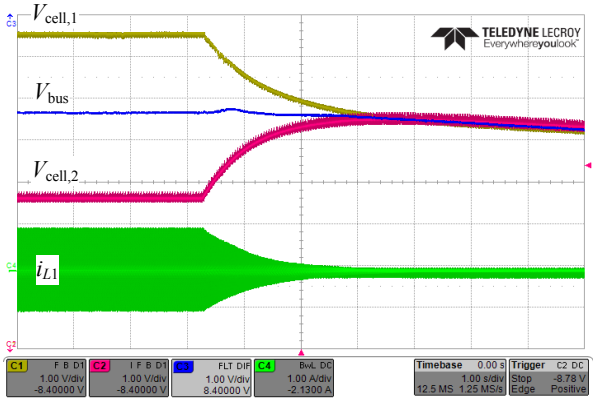

Fig. 12. Convergence of the cells' voltages for the case that $V_{cell,1}$ and $V_{cell,2}$ are preset to 12V and 8V, respectively. C1 – $V_{cell,1}$ (1V/div), C2 – $V_{cell,2}$ (1V/div), C3 - V_{bus} (1V/div), C4 – inductor current i_{L1} (1A/div). Time scale is 1s/div.

changes according to the instantaneous cell's voltages average value, in agreement with (1). Also, the inductor current decreases as the cells' voltages converge and ΔV decreases, as predicted by (6). Convergence of the two cells is depicted in Fig. 12. Also here, after the cells have been balanced, the inductor current reaches zero since ΔV=0.

V. Conclusion

In this work, a new non-isolated balancing topology for serially connected batteries string has been introduced. Fast convergence of the cells is achieved using a parallel balancing approach with low voltage bus capacitor. The new balancing topology uses the adjacent balancing modules when balancing a certain cell. The DCM operation and the fact that no energy circulates in the system when the cells are balanced result in extremely low quiescent power loss. Control of the modules is very simple and does not require any current or voltage sensors to regulate the operation of the system. The theoretical analysis and the results of the experimental prototype showed fast convergence of the cells to negligibly small voltage difference.

Acknowledgements

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