Optimal Design of a Class-E Resonant Driver

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***Abstract*—In many applications of class-E converters, custom made design of the isolation resonant network is impractical and off-shelf products are used. In this case, matching between the target output parameters and converter components requires an additional passive matching network that its parameters are found by a tedious optimization routine. This paper introduces a behavioral modeling based optimization method for class-E resonant converter, which significantly simplifies the component selection procedure. The method reduces the number of unknown variables during a simulation based parameter optimization search. The results of the optimization process are demonstrated on an off line, digitally controlled Class-E, PT based AC/DC converter.**

I. INTRODUCTION

Class-E converters are famous for being a simple and effective solution for many consumer electronic products, RF power amps, and very high-frequency converters [1]. Piezoelectric transformers (PTs) are considered to be advantageous in some power electronic applications due to their relative small size, high insulation properties and potentially low cost. PT applications that were already demonstrated include battery chargers [2], [3], drivers for high side IGBT and MOSFETs [4], feedback isolation [5], fluorescent lamps [6], [7] and LED drivers [8]. Although integration of a PT into a class-E converter may seem attractive in terms of simplicity and cost-effectiveness, it is found to be extremely challenging due to match the stress requirements of the converter and the PT. The example considered in this study, is an off-line PT based power supply that applies a Class-E converter (Fig. 1). If application of custom made PT [9], [10] is impractical from the economic point of view, one may consider the incorporation of matching networks [9], [11] to enable the use of available PT units. However, the design of the matching network and the redesign of the converter elements may pose a considerable engineering challenge due to the interaction between the converter, matching network and PT.

The objective of this study is to develop a simulation based optimization approach that eases the design procedure of isolated class-E resonant drivers. Here, rather than applying an exhaustive multi parameter trial and error simulation, this study applies a novel optimizing procedure that saves simulation time by reducing the number of the unknowns.

II. OPTIMIZATION STRATEGY - REDUCING THE NUMBER OF UNKNOWN VARIABLES

The objective of the proposed simulation based design is to find the values of the two independent parameters L and C_{Div} such that the input voltage to the PT will not exceed the

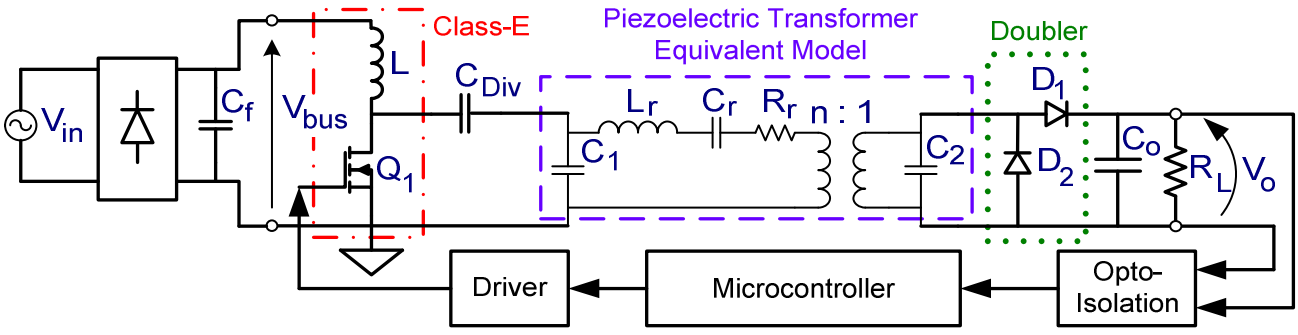

Figure 1. Class-E converter with PT represented by its equivalent model.

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maximum rated voltage and that the switch voltage will not exceed a given maximum value, while maintaining soft-switching and nominal output power over the expected input voltage range. The optimization procedure can be simplified considerably if the search is reduced to one parameter rather than the original two independent variables, L and C_{Div}. Variable elimination is accomplished by a simulation model developed in this study (Fig. 2) in which one of the unknowns (C_{Div} in present case) is adjusted automatically and independently during the search. This is realized in this study by applying a model of a voltage controlled variable capacitor similar to the method described in [12] that is adjusted by a closed feedback loop to maintain the required output current (Fig. 2). The simulation model includes the class-E stage, variable capacitor block, a PT model [13], rectifier, output filter capacitor and the load. The variable capacitor is controlled by a feedback loop that comprises an error amplifier and compensator to limit the bandwidth and assure stability of the loop during simulation as explained in section III.*B*. This feedback loop adjusts capacitor C_{Div} automatically such that the output power is at the desired level. The optimization is done under the assumptions that the system (Fig. 1) will be frequency controlled while the duty ratio is fixed. This simplifies the digital control system since it requires changing only one variable. The down side of a fixed duty ratio is that the maximum switch voltage will be a function of the bus voltage. However, the concept of optimization outlined below can be adopted to optimize the elements' values when the control is carried out by both frequency and duty cycle.

III. Modeling and Control of Simulation Compatible Variable Capacitor

A. Simulation compatible variable capacitor model.

Variable capacitor is required for the design by simulation procedure described in this study. Unfortunately, this element is generally absent from major simulation software packages. To overcome this, a generic and straightforward variable inductor implementation method, as described in [12], is reevaluated and adjusted here to implement a variable capacitor.

The basic concept of the proposed variable capacitor model is to reflect the behavior of a linear capacitor through a nonlinear "transformer". As was suggested in [12], nonlinear transformer can be implemented using two dependent sources, voltage dependent voltage source, E1 and voltage dependent current source, G1. Figure 3 presents the implementation of variable capacitor by reflection via nonlinear "transformer" in OrCAD PSpice. The sources E1 and G1 are defined by:

$$\begin{aligned} E1 &= \frac{V_{sec}}{K} = V_{pr} \\ G1 &= I_{pr} = I_{sec} \end{aligned} \tag{1}$$

where K is the gain coefficient, V_{sec} and I_{sec}, are the voltage and current at the transformer's secondary, respectively. V_{pr} and I_{pr} are the voltage and current at the primary of the transformer, respectively. The impedance, X_{C1}, of the original, constant value capacitance C1 equals to the ratio between its voltage and it's current. The impedance reflected to the primary, X_C', taking into account transformer behavior as described in (1), results in:

$$X_C' = \frac{V_{pr}}{I_{pr}} = \frac{(V_{sec}/K)}{I_{sec}} = \frac{1}{K} \cdot X_{C1} \tag{2}$$

Consequently, the capacitance, C', reflected to the primary side, has the adjustment parameter K, and equals to:

$$C' = K \cdot C1 \tag{3}$$

If K is made dependent on some voltage in the circuit, for example output of a compensator, V(C). This setup will dictate reflected capacitance to the primary of the

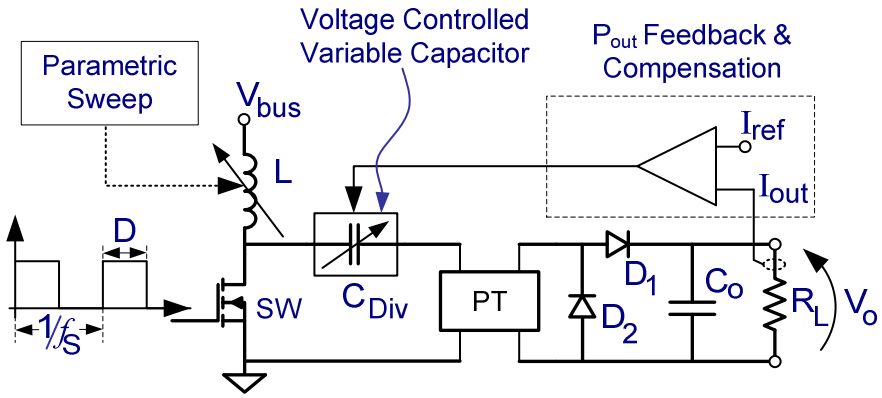


Figure 2. Simulation scheme used to lower the number of unknowns from two to one.

transformer, and in the case of the model in Fig. 3 will emulate a voltage-dependent variable capacitor between the nodes "cap1" and "cap2". The resistor R_{conv} (Fig. 3) is added to avoid the convergence problems of the numerical simulator.

B. *Automatic control of variable capacitor.*

Automatic search for C_{Div} value to keep the output current constant is accomplished by a closed-loop setup that follows the control diagram of Fig. 4. The variable under control is the output current, S_O, which is compared to the reference value, S_{ref}. The resultant error signal, S_e, is fed into a compensator, which produces a control command signal S_C. The role of the compensator here is to allow the output current to converge into the desired value governed by the reference. The compensation signal, S_C, is fed into a block named "Variable Capacitor". This block is a linear unit translator, from S_C, which may be in volts, or unit-less variable, to C, which represents Farads (coded into voltage for simulation purposes). Finally, the power stage accepts three inputs: D – constant duty cycle, L – inductance value which is a sweep variable as will be explained in section IV.*B*, and C – the capacitance that is automatically adjusted by the feedback loop.

It should be noted that in order to regulate the output power at its nominal value, the control variable that is required is the output power. However, due to the resistive load configuration (Fig.1), output power control can be obtained by regulation of the output current.

IV. PT DRIVER OPTIMIZATION

A. *Selecting the initial values.*

The operating frequency range of the system is selected to be to the left of the natural PT resonance frequency. The initial maximum switching frequency is set according to the transfer function of the bare PT. To avoid operation at the resonant frequency, the maximum frequency is selected to be at a transfer ratio point which is 5 to 10 percent lower than the peak transfer ratio. Initial duty cycle is set to be 50%. Since C_{Div} is forming a capacitive voltage divider with the PT input capacitance, the simulation based search boundaries were chosen to be a decade above and decade below the PT input capacitance value. The inductance is a sweep parameter in the simulation. The inductance sweep range is

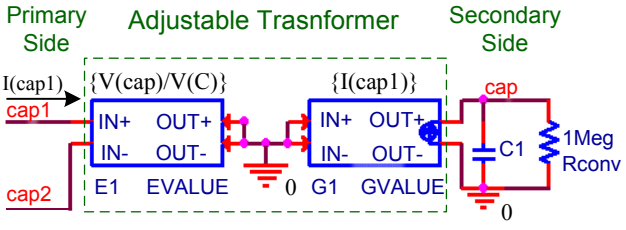


Figure 3. Variable Capacitor implementation in OrCAD PSpice.

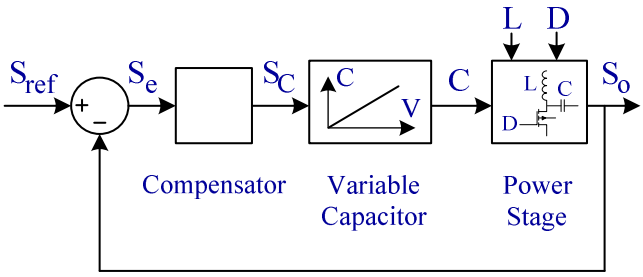


Figure 4. Automatic capacitance adjustment control diagram.

set to be around the value that will resonate with C_{Div} at the PT resonant frequency. Transient simulation run time is set such that the value of the variable capacitor is allowed to converge and stabilize.

B. *The simulation procedure.*

Simulation begins by testing the "worst case" boundary, namely, setting the input voltage to the minimum and the switching frequency to the maximum values, respectively. Transient simulations are run in parametric mode, sweeping the inductor's value. Performance analysis option (in PSpice) is then used to examine the maximum voltages across the switch, ZVS condition and the maximum voltage on the PT. Since the chosen control is based on fixed duty cycle, the maximum voltage across the switch is approximately proportional to the input voltage. Therefore, the observed maximum voltage on the switch, for simulations with low input voltage, should not exceed the value of the specified maximum switch voltage divided by the ratio of maximum to minimum input voltages:

$$V_{sw(max)}^{Low} = V_{sw(max)}^{High} \cdot \frac{V_{bus}^{Low}}{V_{bus}^{High}} \qquad (4)$$

where the upper script defines Lower/Higher live voltage limit and the subscript defines the measurement point, either bus – bus voltage, or sw(max) – maximum voltage across the switch . If there are no points fulfilling these conditions, the "ON" time of the switch is reduced, and the simulation is run again. This procedure is repeated until an inductor-capacitor pair and the "ON" time satisfy the requirements for zero voltage switching, maximum voltage across the switch, maximum PT voltage and nominal output power.

Following the initial stage outlined above, a simulation of the transfer ratio of the system as a function of the switching frequency is carried out. It should be noted that the system's response and peak location could be significantly different from that of the bare PT. Even so, the maximum operating frequency should always be chosen around the peak response of the PT to ensure high efficiency [13]. The more accurate transfer function can then be used to select again the maximum switching frequency. Typical simulation results are shown in Fig. 5.

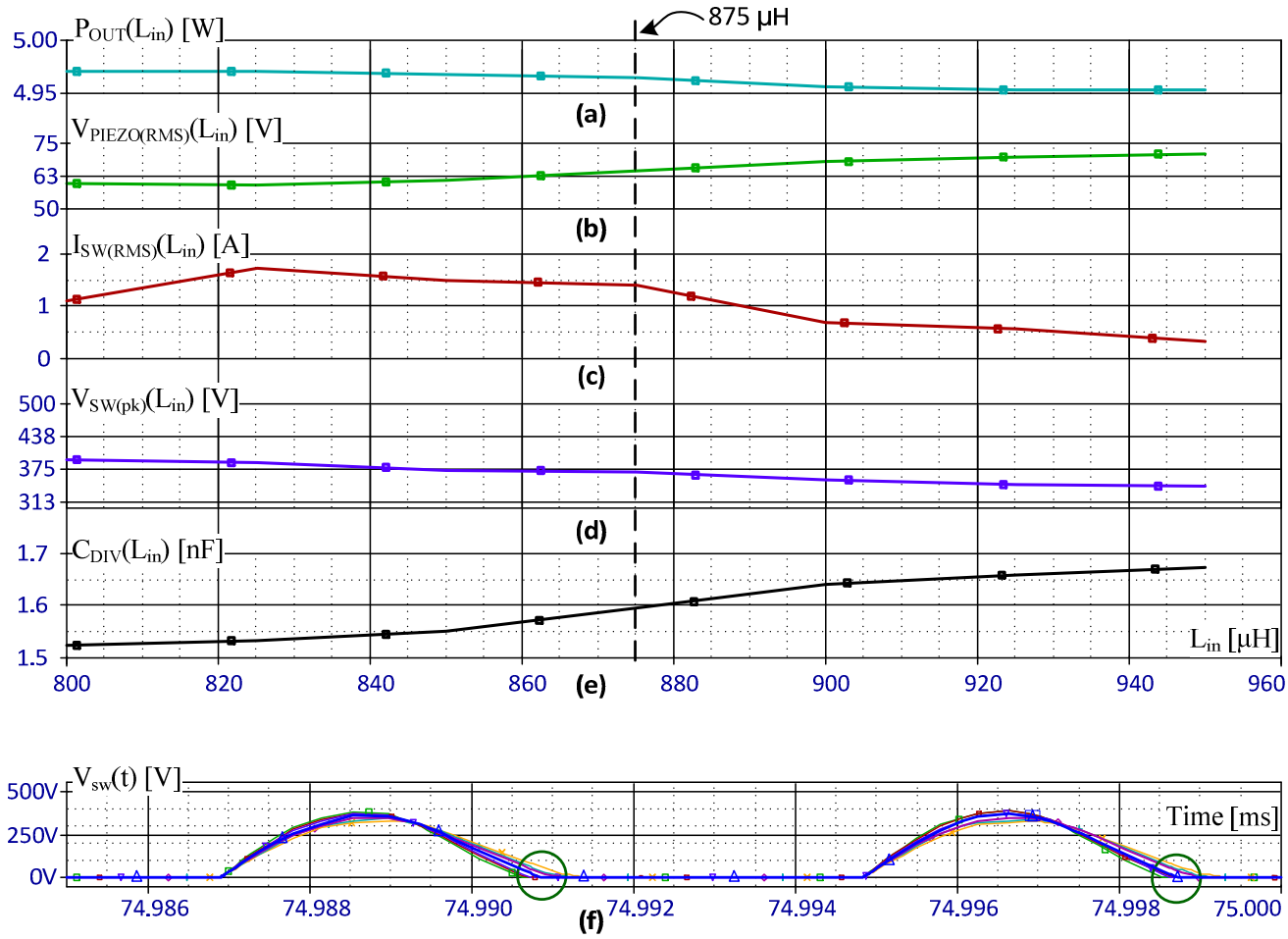


Figure 5. Simulation results of driver optimization procedure. Performance analysis (x axis is an inductor value):
(a) Output power, (b) Maximum RMS voltage at the piezo input terminals,
(c) Maximum RMS current through the switch, (d) Maximum voltage stress across the switch,
(e) Capacitance value of C_{Div}, as converged by the automatic capacitor search feedback loop.
(f) Time waveform: voltage across the switch (multiple traces obtained from parametric sweep simulation (inductance as the sweep variable), bold trace is the system performance with 875µH inductor).

V. Simulation and Experiment

The proposed computer aided design and optimization method was tested on the prototype depicted in Fig. 1. The approximate parameters of the PT (PTA005010, Konghong Co. Ltd., China) equivalent circuit model were determined by the method described in [14], and found to be: L_r = 2.544 mH, C_r = 792 pF, R_r = 31 Ω, C_1 = 3.6 nF, C_2 = 75 nF, n = 5.6. Output circuit components were: C_O = 470 µF, nominal load R_L = 80 Ω and two schottky diodes (MBR340) D_1 & D_2

Input rectification stage and filter capacitor C_f were designed to supply V_{bus} with maximum ripple of 5 V_{p-p} under the nominal load, switch with R_{ds-on} of 0.75 Ω was employed. Output voltage was controlled to be 20 V, and the nominal output power was 5W.

The circuit optimization procedure was carried out to comply with the requirements of the system, as summarized in Table I, and the results are presented in Fig. 5. As can be observed, the compensation network adjusts the variable capacitor to such that the output power is close to the target of 5W throughout the simulation range (Fig. 5a). The second optimization constraint is the maximum allowable rms PT input voltage, which according to the system requirements (Table I) needs to be below 65V, i.e. the maximum inductance for this case is below 880µH (Fig. 5b). Figs. 5c and 5d show the expected rms current through the switch and the peak voltage across the switch, respectively. Both are evaluated versus the system requirements. The maximum allowable voltage is 600V, but this voltage will appear at the higher end of the input voltages range. At lower end the

limit, according to (4), was calculated to be 353V. According to Fig. 5d, the inductance required to satisfy the performance goals should be larger than 870µH.

Given the set of constraints outlined above, the optimal value of the inductor was found to be L = 875 µH. The inductance selection is highlighted with a bold dashed vertical line in Fig. 5. The paired capacitance is extracted from Fig. 5e to be C_{Div} = 1.6 nF. ZVS can be evaluated from the time domain switch waveform of Fig. 5f. The correct trace for the selected inductor is highlighted in bold (blue), and the relevant ZVS evaluation area is marked with green circles. The (fixed) duty cycle required to assure proper operation over the input line voltage range, was evaluated to be around 35 %. The final operation range was found to be 126 kHz for V_{bus}=110V, and 120 kHz for V_{bus}= 187V. The control task was implemented by TI's ultra-low power microcontroller MSP430F2013.

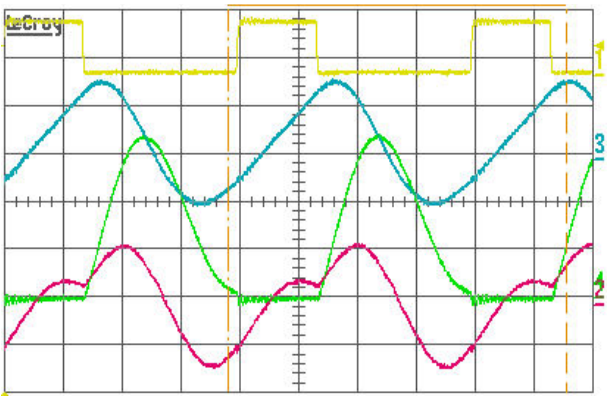
Figure 6 presents experimental waveforms of the laboratory prototype, and the capability of the system to comply with the full input voltage range, from 80 to 132 Vrms. Figure 6a presents the operation under the lowest input voltage and highest switching frequency conditions. ZVS can be observed, and the maximum voltage across the switch is around 350V as calculated above. The operation at nominal conditions is shown in Fig. 6b. Operation under highest voltage stress is depicted in Fig. 6c. In this case the line voltage is at its allowed maximum value and the switching frequency used is reduced to the lower limit. As one can see the maximum switch voltage is around the allowable limit that was specified.

VI. Discussion and Conclusions

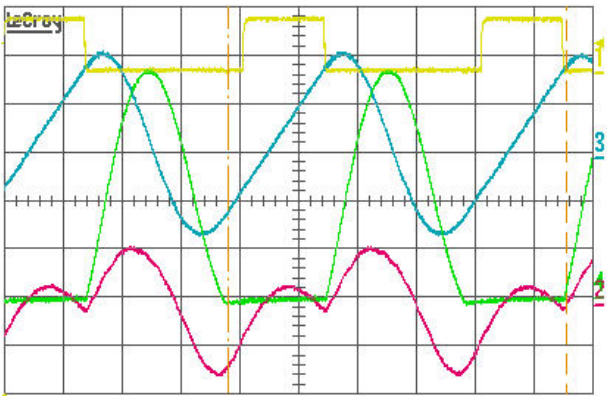
A computer aided design of an off-line, digitally controlled Class-E PT converter was carried out by applying a new simulation approach. The proposed advanced simulation procedure simplifies the search of unknown parameters by reducing the number of unknown variables from two to one. This is accomplished by an auxiliary feedback loop used during the simulation runs, and adjusts the value of one of the unknowns (a capacitor in the illustrated case) such as to maintain the desired output power. A step-by-step simulation procedure is then used to determine the optimal value of the unknown parameter (the value of an inductance in present case) such that the design objectives are met. The converter prototype designed using proposed method was found to comply with the requirements of ZVS operation, delivery of nominal power and maintaining safe switch and PT voltage, over the grid range of 80 Vrms to 132 Vrms. Even though demonstrated for the case of a Class-E PT driver design, the proposed method of variable elimination could be useful in other simulation based designs.

TABLE I. Design Example: System Requirements

V_{in} [V_{rms}]	V_{bus} [V]	V_o [V]	P_o Nominal [W]	V_{sw} (Max) [V]	f_s [kHz]	V_{PT} (Max) [V_{rms}]
80-132	110-187	20	5	600	100-150	65



(a)



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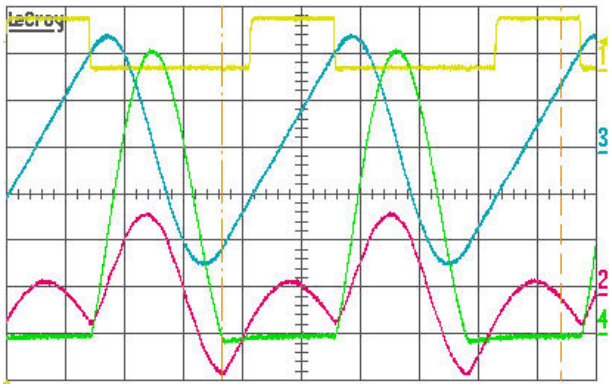

(c)

Figure 6. Experimental results; Bus voltage condition: (a) Lowest, (b) Nominal, (c) Highest; Time 2µS/Div; Traces (from bottom to top): (2) PT input voltage 50V/Div; (4) V_{sw} 100V/Div; (3) I_L 0.2A/Div; (1) Gate signal.

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